

Date – 9/07/2010

Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Carl Barnhart, Craig Stephan, Adam Cron, Francisco Russi, Adam Ley, Carol Pyron,

Missing with pre-excuse: Wim Driessen, Ken Parker,

Missing: Neil Jacobson, Ted Eaton, Heiko Ehrenberg, Dave Dubberke, Roland Latvala, Bill Eklow,

Agenda:

Review current Draft updates and get feedback

Minutes:

Meeting called to order at 11:04 am EST

Review of latest draft changes:

Input spec element now describes a Float or a Pull

Figure B.7 and B.8 updated

Section 13/14 – breaking out rules that are specific to register itself vs instruction

(B.8) Breaking out register mnemonic description/ register fields descriptions/ register field association descriptions.

Goal is to describe without the package information.

(B.10) Broke out user-supplied VHDL package information into 2 sections for boundary register cell and internal registers.

Did this to clarify for the Register descriptions.

Question on bracket type in BNF ([] or { }) for mnemonic identification statement/register fields statement/register_fields_association_statement

Carl - What is the problem with allowing Multiples?

Adam L - seems that we are already going to have to deal in the tools with multiples of these statements either from multiple packages or in BSDL

CJ – from a compiler tools point of view it doesn't matter.

CJ – will go back and look and see what the right answer is. Do it either way.

Would prefer to see only one (use [])

(B.8.12) Optional Device register description.

(b.8.1) Overall Structure of the Entity Description

Another question of [] vs { }

Top level BSDL file.

Carl – probably multiple copies of attribute there.

CJ – descriptions seem to be a single use.

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Maybe the {} give you ability to cut and paste.

Adam L - More of a programmatic than a manual cut and paste. But that is applicable. Makes it easier to add things without having to make sure that you have terminated the statements/strings properly

Carl – Curious why there is only 1 design warning?

Adam L – that is the way it has always been. 1 string that you can put as much as you want in there.

Carl – this probably reinforces CJ’s argument.

CJ – doesn’t have a preference but wants to do it the way the group wants,

Isn’t consistent and doesn’t want to have a problem later

Francisco would like to see multiple design warnings

CJ – due to the high work load - If it doesn’t need to be fixed than would prefer not to fix it.

(B.8.18) Register Fields

Syntax changes based on package.

<package_object> ::= < package_name>:package is the difference

user package_body is needed

Blank package_body when you have mnemonics and fields

(b.10.3) example needed to explain this

(B.12) is weak and in need of some reinforcement

Table B.11 – Legal Capture Sources for <cell context> of OO

Updated table

CJ –is it incorrect using L? Should we be using A?

Carl – should all be A’s

(definition of “A” and “L” are in section B.10.2.2.1 of current draft)

Adam L – no. they may need to change for other types. For conventional

Observe -Only they are correct. Doesn’t agree with change.

CJ – went through the discovery of how OO meant input without update cell.

OO was inserted so we can observe differentials.

Observe – Only vs Observe_Only

Adam L – is it really worth putting it back. Do we want to create a new cell type such as the ROO and deprecate the use of the OO. If it applies only to ROO than yes A is correct for Table B.11.

CJ – we have OO that are ROO’s. At the point where the ROO is clearly called a redundant cell and defined that way.

OO is something you can have on the single side of the Differential, but that isn’t allowed in 2011 version. For the user that is the one place that would be different.

Carl – BSDL from Carol, every input was an OO.

CJ – that is what got us down this path

CJ – back to the original intent of OO and no longer confused with being an input

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Carol – standard says that input without control function is an OO?
Carl – BSDL function is properly INPUT. Don't have to have a control cell for input

Carol – only the differentials were OO. Regular pins were inputs/outputs/bidir
Term OO has had multiple meanings and is confusing.
CJ - that has been the problem. I think we are ok now.

Carol – on discussion of { } vs [] – thinks we can get by with [] . When we were working through the examples she didn't feel a need for multiple attributes.

Carl – simplifies putting it all together

Carol – not that hard to incorporate it all into one attribute even if you are cutting and pasting

CJ – Would like to know if Freescale has a device that we could use for an example. This would make the example section more up to date.

Not just a snippet of code but a full device.

Carol – if you are looking for a real device at ballot time, nothing would be ready by then. And there would be 30 pages of BSDL. She may have a part that could be available, but it would not be a small example.

CJ comments that there are more changes than what has been discussed so please continue the review.

(9) Specifications of Test Data Register

init_data and init_status added

Recommendations – added recommendation to add test data register to be accessed by a single instruction in order that they can be used with PDL. Wording here needs to be explored.

Don't want PDL to be like BSDL. Don't want to see PDL create rules about architecture.

If you have a TDR that you want to use in PDL you can only have a single instruction.

Recommendation here and then in annex c have a single instruction.

Group concurs

Working Group Meeting on 9/14/2010 will be canceled due to conflicts. Friday's Tiger Team meetings will continue.

Working Group Meetings will resume on 9/21/2010

* Carol will be out for next meeting (9/21)

Meeting adjourned: 12:15 EST.

Next Meeting: 9/21/2010 11:00 AM EST

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.

1. Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.