

Date – 9/28/2010

Attendees: CJ Clark, Bill Tuthill, Carl Barnhart, Ken Parker, Craig Stephan, Adam Ley, Adam Cron, Brian Turmelle, Wim Driessen, Heiko Ehrenberg, Francisco Russi, Carol Pyron, Lee Whetsel, , Roland Latvala,

Missing with pre-excuse:

Missing:, Dave Dubberke, Neil Jacobson, Ted Eaton, Bill Eklow,

Agenda:

Continue discussion about init-restore/init-clamp

Meeting Called to order at 11:13 am EST

Minutes:

INIT_RESET

KPP – envisioned something called RESTORE.

Similar to the Master RESET line on a device.

Could write RESTORE instruction into TAP to initiate RESET of the IC

Private instruction in such that we didn't tell what it did but would invoke RESET condition. That is all we would specify. Would not specify what the exact RESTORE sequence is. Leave that to the designer.

CJ – what would the rules be for this instruction?

KPP – Designer would specify OPCODE and connect it to the master reset pin. If you supply a RESTORE instruction

Carl – would you allow a TDR for multiple resets?

KPP – don't see why not. Left to the designer. It is a way to get at the reset functions in a TAP based way.

CJ – need a way to communicate which bits reset what? Do we end up with an INIT_RESTORE that is in PDL?

KPP – we could if you want to go that far?

CJ – complex devices still have a single reset pin.

CJ – what are the purpose for multiple resets?

Carl – different levels of reset is one thing. Multiple cores is a another possible reason.

Adam C – reset conditions are different based on how pins can be set.

Francisco – sees 2 groups of reset. Global and local.

KPP –is trying to get a handle on where the industry with needing this function.

CJ – Looking to perform a reset that is similar to power on reset.

CJ – Carol's chip would power up and then run INIT_SETUP to program IOs.

Carol – thought reset/restore was after you complete tests.

CJ – no guarantee that chip would boot up correctly

If we did init RESTORE and then a board test you would have to do an INIT SETUP again to run those tests.

Carol – why call instruction INIT RESET?

KPP – name keeps changing. Thought of it as the back-stop to the init process.

RESTORE would be same as pressing reset button.

Carol – how do we de-assert reset? While reset is asserted there is no functionality.

KPP – use RUNTESTIDLE to hold RESET active and then when leaving RUNTEST de-assert reset

CJ – how do we communicate this to the test engineer?

Carl – chip designers have been doing this function for a long time. But no consistency, that no one has tried to standardize this. Opposed to this because it is already done and not a standard process once reset is asserted. All the standard is doing is giving a name.

KPP – we could put some rules on it. How long you need to assert/de-assert. Allow a register with options. Or just a push button reset

Carl – test engineer without documentation from designer doesn't know how to use it.

There is too much data that needs to be communicated and concerned the designers would just think of the RESET as a standard and not document it

CJ – There are complex chips and chips with area gray about how much boot up has occurred.

Large number of devices today that have a single reset pin on that device. The aim of this instruction would be to issue a RESET that is the same as this pin. This would have a large benefit to the industry.

Carol – never had a JTAG reset command. Just toggled a physical pin.

Would be relatively easy to have the same effect as the physical pin.

Toggling the pin is not a full POR. You have to do a sequential set of POR operations to start boot up sequence.

CJ – Industry is begging for an instruction that emulates the pin toggle for RESET.

Define the instruction as equivalent to toggling the RESET pin.

Carol – restarting a boards boot process? This would be difficult as it is a broad scope.

KPP – could be too grandiose of an idea.

Carol – need to have system clock to lock PLL.

KPP – INIT RESET would start a train of events. May or may not provide all the events needed to start up.

CJ – Carols' point is restarting boot process is a little far reaching.

Want to define it more as a way to reset the IC.

KPP – would agree with that.

Carol – want to explicitly state as a rule that it doesn't toggle the TRST

CJ – assumed that it would not mean the TRST

Carol – This is to be a mission mode reset.

Adam – when you have a POR that is not a separate pin, when that is feeding the TRST, would you want a separate path. Do you want to reset the TAP.

CJ – Figure 6.8 shows both. Don't see that as a problem.

Update the restore instruction go to runtest idle and then go to TestLogicReset.

After some period of time in runtestidle put it in to TestLogicReset.

Carol –

CJ – simply say that the tap is in the TLR after the instruction and wait period.

KPP – want to make sure that there isn't a new arrow in the state diagram that goes from RuntestIdle and then to TLR.

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CJ – no new arrow. Concern that the POR of the system can be tied to tap controller reset. So reset would occur and put TAP in TLR state

KPP – chain can be broken if only one device goes to TLR while other devices that don't have RESTORE instruction would be in runTestIdle.

Adam – can happen with pins. Have to understand to use the controller to move the chains back in sync. Use a TMS reset.

KPP – RESTORE is last thing you do. Do simultaneously and then sync up the other devices with TMS reset.

CJ – Do INIT RESET, wouldn't go to reset. After you issue the INIT RESET the safest route would be to issue a TMS reset to synchronize your TAPS

Carol – is it a permission or a requirement to reset TAP?

CJ – want one way or another? No need to do it both ways.

Carol – votes to not reset the TAP.

Adam C – feels that this would be creating a burden to disconnect the POR from the TRST.

CJ – if you reuse the POR like figure 6.8 you are adding extra work to separate that out.

Carol – master POR reset has no effect on TAP on Freescale parts.

CJ – but you have a TRST pin

Carol – right, maybe the rule is reset the tap if you have the TRST pin and not if you don't

CJ – simply, the reset line internally you will simply AND that signal going into the TAP
Much safer to reset the TAP

Carol – doesn't want to reset tap because there are many switches inside the chip that will over ride thing.

Carol - in a chip debug environment we would not want to reset everything. In a board environment you would.

Carl – Are we talking about board level of POR or chip level.

CJ – Chip level only. Figure 6.8 is only for internal POR.

Carl – POR and TRST signals have been kept separate.

CJ – it is still like that but we have a flip flop that is clamping the pin.

Carol – standard only mandates this if the TRST signal is not present.

CJ – both are allowed (POR and TRST pin) to clear flop.

Carol – POR is optional if TRST*.

CJ – any input on INIT_RESET vs. INIT_RESTORE.

Lee- concern about scheduling when the chips go into RESET? Some systems may come up before others. Would this cause a problem.

CJ – intent would be to issue reset command simultaneously.

Lee – some chips may respond to reset faster than others and could have domino effect

CJ – designers should have accounted for this as it is the same as yanking on the reset line.

Lee – complex chips may not be as easy. System level can fix itself

CJ – all this instruction does is emulate toggling the reset pin of the chip internally.. not specifying sequence of what happens when reset is asserted in chip.

Lee – Causing the Test Reset to occur when RESET instruction is called, this could cause some problems with on chip instruments when trying to monitor what happens at reset. If

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we force the tap into reset when we issue this instruction, you wouldn't be able to continue communicating with the instrument.

Lee – 2 different options for RESET. Full reset that doesn't reset the tap or a functional Reset that doesn't reset TAP.

Meeting adjourned: 12:11 EST.

Next Meeting: 9/28/2010 11:00 AM EST

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.

- 1 Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.