Date – 11/09/2010

Attendees: CJ Clark, Bill Tuthill, Ken Parker, Dave Dubberke, Adam Cron, Carol Pyron, Adam Ley, Craig Stephan, Carl Barnhart, Brian Turmelle, Francisco Russi, Lee Whetsel,

Missing with pre-excuse

Missing : Wim Driessen, Roland Latvala, Ted Eaton, Neil Jacobson, Bill Eklow, Heiko Ehrenberg,

Agenda:

1) Report on input from ITC
2) Other WG member inputs
3) More init_clamp/ic_reset/lobotomy problem

Meeting Called to order at 11:08 am EST

Minutes:
ITC summary
CJ – Sent out poster from poster session in email
CJ – in general during poster session there was a lot of good input from attendees. Everybody in general was happy to see what the group was doing.
KPP – a lot of interest in all the Different 1149 -DOT Standards. All got a lot of attention
CJ – heard good input on Clamp Hold as well.

Feedback from ITC

John Siebold from TI mentioned that they would like to do configuration through Boundary Register. Can INITDATA be described as the boundary register?
Adam – how do you persist the init values during EXTEST
Carl - Software would have to reload values
Carol – had discussed this earlier decided it was not a good idea. Not sure if it was forbidden.
KPP- concerned it would be a long register
Carl – architecture doesn't make sense. For every set up change you would need a new BSDL
CJ – use register fields attributes to call out bits. But seems like an ADHOC approach to solve problem. Wouldn't be compliant with INIT SET

John's concern was routing.

Carol – Believes he is looking at current implementation. Not a common implementation across all chips.
CJ – better to create a better solution than try to change standard to something that was already done

Lobotomized IC

CJ - Ken's concern is that Reset pin will not clear the device.
Carl – if you are in test mode than the reset pin is not connected to the internal logic
CJ – if it is a BC_4 the reset is going to the chip
Carl – if you use that. But that is not what everyone does.. Carol's resets are monitored. You are describing a reset that can override JTAG and not everyone does that. In the past you do a TRST you expect it to work. But in ClampHold you can't count on the reset to take the chip out of test mode. JTAG is supposed to be a higher priority than functional (includes reset)
KPP– would have to include reset as a compliance enable if you want reset to be part of JTAG .
Carol - Once in ClampHold state you can always release it with another serial sequence. For TRST pins it is trivial, but for people that don't have the TRST pin available than it is more difficult.
CJ – lobotomy problem described is that we go back to bypass or device id the chip is in a lobotomized state. Reset state clears the device. Other people see it the same way.
Adam C – are we talking about TRST or system Reset.
CJ – System Reset.. System Reset clears the chip. From Ken's paper, when we go into EXTEST when we are done we leave the chip in a funky state. The way we have been avoiding the problem we power down or yank on system reset pin.
KPP – engineering problem to determine how to get the chip out of the lobotomized state and back to normal. Might be an order reset pins need to be pulsed. Or one key reset pin to toggle. Not easily understood if you were just given the schematics and no assistance.
CJ – you have to at some point stop testing.
KPP – agreed. And turning off the power is legitimate if it can be done before something bad happens. But in general concerned about time when testing starts and power is still applied.. What is that board going to do to itself? No one understands exactly what the bad things are for a board.
CJ – currently we have a mixed of devices, holding the board with reset low was always considered a safe state. Is it safer to have Clamp Hold persistent so some stay in ClampHold while others go into reset?

KPP – hoping to give people tools that they can use for test. If there is a better way to take care of the boards issues than ClampHold than use it.

KPP – have talked about having ClampHold with options on it (via a register)
CJ – Original concept of ClampHold was to support in-sitchu on chip test. If you add more complexity, concerned we don't' get what we want for on chip in-sitchu test because it is getting overloaded with extra complexity to take care of a board test problem. Doesn't want to lose the in-sitchu test to fly and be available.

Adam – Carl started a thread with 2 bits for the setting of ClampHold functionality. Continue spec'ing ClampHold for what we need and at the end we may have a better idea of whether these issues are real issues.

CJ – are people going to be comfortable implementing this without proper safe guards? Even if lack safe guards is only perceived it may deter people from using ClampHold
Adam L – objects to having TRST to clear ClampHold. TRST should only be used to precondition a chip at POR
Carol – disagrees with that. TRST is used to get back to functional state in JTAG.
Adam L – fine at a chip level. Problematic at board level. Only chips with TRST respond to that stimulus.
Carol – board tools have been dealing with that for eons and doing ok.
Adam L – TRST has to clear the Sticky Bit on ClampHold. Board level context we shouldn't promote TRST for that purpose. Total Test state needs to be cleared by TRST. We should not encourage the use for TRST other than power on reset at the board level.
CJ – at board level we would like to clear that bit at the board level when it exists. If we can do ClampRelease then we don't need to toggle that bit.
Agree. And only offering TRST to clear that bit or instruction is where concern is. Behind having bypass to allow you to clear the bit
Carol – clamp release is good. Need to have both instructions for clamp hold.
On the fence for bypass/id clearing clamp hold.
KPP – scenario for all 1's is if TDI breaks and all we can get is a stream of 1's into chip to clear clamp hold.
Adam C – bypass state allows you to reset the device by other means.
Kpp – would have to think about that. Boundary cell that is attached to TRST has extra qualifier
CJ – meant system reset?
Adam C – yes – System Reset.
CJ – We want to consciously load the state bypass or id and that clears the sticky bit.
Embedded system we have devices that come in and out of the scan chain.
Adam C - Need to at least get to update.
CJ – yes. Meant shifting long stream of IR and obviously go through update and back to idle. By allowing bypass to clear it, no matter how long the scan chain is everything is back into mission mode and with bypass you don't need to know the length of the chain.
KPP – action of loading through update IR would clear the sticky bit. No bypass if passing through TLR?
CJ – correct if sticky bit is on. Reset output of tap controller is blocking to instruction state machine
Adam L – how do you describe to the tools that they will not be shifting the bypass register.
CJ - you would be able to shift bypass.
Adam L – clamp hold creates a parallel state diagram once sticky bit is set. In parallel diagram mode is stuck but all other functions are working.
Carl – TLR state needs to be redefined in this alternate state diagram. Have 17 states not 16.
Carl – this is adding complexity to dot 1

Meeting adjourned: 12:12 EST.

Next Meeting: 11/16/2010 11:00 AM EST

NOTES:

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.

1 Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.

Weekly 1149.1 Meeting coordinates

1. Please join my meeting.
https://www1.gotomeeting.com/join/172495048

United States: +1 516 453 0012
Meeting ID: 172-495-048
Audio PIN: Shown after joining the meeting

2. Other call in numbers
Australia: +61 (0) 8 6365 4094
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