# Date - 12/21/2010

**Attendees**: CJ Clark, Bill Tuthill, Ken Parker, Adam Ley, Carl Barnhart, Craig Stephan, Heiko Ehrenberg, Wim Driessen, Carol Pyron, Brian Turmelle, Roland Latvala, Ted Eaton, Bill Eklow, Adam Cron,

# Missing with pre-excuse

**Missing:** Dave Dubberke, Mike Richettie, Francisco Russi, Lee Whetsel, Neil Jacobson,

# Agenda:

1) Required Patent Disclosure Slides (2:00)

# Everyone at last meeting agreed that they read and understood obligation

- 2) Election formalities-discussion (15:00)
- 3) Dec 28<sup>th</sup> meeting? (5:00)
- 4) Review/Discuss IC\_RESET
- 5) New Business

# Meeting Called to order at 11:02 am EST

#### Minutes:

Reviewed Patent Disclosure Slide

Review election Results
CJ - Chair
Carol - Vice Chair
Carl - Editor
Bill T - Secretary

Officers need to be IEEE/SA members CJ, Bill, and Carl are members

Carl has some problems writing to PDF Ted volunteered to help Carl export files to PDF. Carl will resolve issue writing to PDF Dec 28<sup>th</sup> meeting

Carl makes motion to cancel Dec 28<sup>th</sup> meeting. KPP seconds

None opposed. Motion carries.

Dec 28<sup>th</sup> Meeting has been canceled.

Ken points out that meeting notices are not scheduled after Jan 1. CJ will need to reissue meeting notice

#### IC RESET

Permissions

Carl - Remove permission f) based on input from Ted.

Ted – can still be a permission but made a "may" rather than "should"

Carl - g) and h) no comments to be had on these 2

Reset-select register

New clause

Carl – Rule does not require an update flop.

Carl – with Ted's addition it will require an update flop

CJ – agrees

Carl – basic point of rule is that it is a minimum 1 bit.

Carl – changed rule a)

KPP – suggests reset select register

CJ – doesn't think "stages" is the right word

Carl – b) is this required any longer? To protect Run Test Idle

Ted – Doesn't see why it would be required

CJ – each one of the bits is like an "and"

Ted – not sure why TLR won't reset that. Not sure why it needs to be all 0's

CJ – might be a mistake. If we can manage the resets better and we are in Clamp Hold and trying to execute something on chip , wouldn't want entering TLR to change anything on the chip.

CJ – CH is optional. Can have IC reset without CH. Seems like we are setting this up to clear bits in TLR and not sure why we would do that.

Ted – because they have to be cleared by reset. Are we separating the TRST Pin and the TLR state?

Carl – Rephrased rule b)

Ted – Where is separation of TRST and TLR State

Carl – TRST is a powerup initialization function. Will reset all of the test logic Once we are operating if you have the clamp persistence controller in the ON state, a number of resets under TLR don't occur.

Ted – in the absence of Clamp persistence where is it separated?

Carl – yes.. in that case it is the same.

Ted – thinks we would be better off separating the TRST pin and the TLR state and define what this would do for both of them.

Carl – lets defer to an email discussion.

CJ – wants to make sure that people can use TRST without Clamp Hold. And make sure it makes sense when to clear

Carl – Rule c) ok

Permission d) Carol wants the ability for decodes here

Ken – this is a function of what the designer wants to do. Shouldn't disallow it.

Carl – permission e) Do we want this.

Ken – perfectly acceptable.

11:30 – Carl had to leave earlier.

Discussion on Editor

CJ wants to add to draft

Ted – other working groups you would edit the section and pass to Editor.

Ken – sees Carl as the interface to the IEEE. And it's up to Carl on work to be done.

New Business

Ken – making good progress. Can we summarize that we have 5 new instructions.

These instructions will be a major contribution for this working group.

CJ - ves.

Ken has been working with Carl on improved figures.

CJ – there really shouldn't be files submitted to the Editor without going to the reflector?

Ken – figure 6.3 thru 6.6

CJ – what would be appropriate would be to share with the working group rather than just handing to Editor.

Ken – in general the working group is the final check off for any change.

Ken shows the group the updated figures.

CJ – what is the IEEE position on the FlipFlop

KPP – The symbol?

CJ – yes they have rules on 2 different ways of showing the logic.

KPP – lay that on Carl. Might want to run it by the IEEE. Symbols in these figures were used in previous standards.

CJ – thinks we should have a figure to show a non gated clock method showing states.

Few members don't like the gated TCK figure.

KPP – just translated from pervious figure. Didn't make any logical changes.

If someone wants a change than he will defer to that person

CJ – wouldn't be a bad idea to add another figure

KPP – that would be a contribution to the standard

CJ – send him the -5 figure and he will modify it for the state.

CJ – No more business.

Meeting for Dec 28<sup>th</sup> is canceled due to the Holidays and lack of sufficient member availability.

Next meeting will be on January 4<sup>th</sup> 2011

KPP – moves to adjourn Seconded

Meeting adjourned: 11:45 EST.

Next Meeting: 1/04/2011 11:00 AM EST

### NOTES:

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

# Current Issues listed and who will champion that issue.

- 1 Observe only. Ken and Carl
- 1. Directionality linkage. CJ
- 2. Power Pins. Heiko
- 3. Pairing power pins with functional I/O CJ
- 4. Sample / Capture. Carol (Freescale) & Roland
- 5. TRST included in PCB level diagram. Adam L.
- 6. Slow to Fall/Rise signaling issue CJ
- 7. "No Connect" Ken and Francisco.
- 8. Device ID Still needs work
- 9. Low-Voltage self observe shorts coverage problem JJ & Intel
- 10. Init Carol & Carl

#### **Action Items:**

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.

Weekly 1149.1 Meeting coordinates

1. Please join my meeting.

https://www1.gotomeeting.com/join/172495048

# IEEE 1149.1- 2011 Boundary Scan Working Group Minutes

United States: +1 516 453 0012

Meeting ID: 172-495-048

Audio PIN: Shown after joining the meeting

2. Other call in numbers Australia: +61 (0) 8 6365 4094 Canada: +1 416 800 9290 Germany: +49 (0) 898 7806 6462

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