

Date – 01/25/2011

Attendees: CJ Clark, Bill Tuthill, Adam Cron, Craig Stephan, , Ken Parker, Carl Barnhart, Dave Dubberke, Wim Driessen, Brian Turmelle, Heiko Ehrenberg, Carol Pyron, Ted Eaton, Mike Richettie, Francisco Russi, Roland Latvala,

Missing with pre-excuse

Missing: John Braden, Lee Whetsel, Neil Jacobson, Bill Eklow, Adam Ley,

Agenda:

- 1) Required Patent Disclosure Slide
- 2) Editor Status
 - a.) Update on web
 - b.) Input on new draft
- 3) IC_RESET – new figures/strawman
 1. Friday my action item was to fix-up/improve figures for reset-select. I have not finished with the Visio drawings yet (just back from holiday, will be ready for Friday).
 2. Carl’s action item to revise/update text of strawman.
 3. Other?
- 4) New Business

Meeting Called to order at 11:00 am EST

Minutes:

Patent Slide shown and reviewed

Reminder of discussion etiquettes

No personal attacks

Let others have a chance to voice their opinion

CJ has 2 comments on current PDF

CJ – Need hyperlink in PDF

Carl – current PDF writer doesn’t support hyperlinks and is looking for another software package. Is aware of the problem and will resolve it as soon as possible.

CJ – Difference docs need to be done

Carl – will post clean doc and do December to January diff and will be posted shortly.

Carl Presented text from the draft on IC_RESET instruction

Minor changes in descriptive text

Discussion moves to Reset_Select register

Carl Will replace RESET_SELECT register figure. Needs more detail for labeling.

CJ will provide a better figure with more detail.

Using Reset-Source rather than Reset-pin. Source doesn't need to be pin, could be internal.

CJ did send out updated figure in document where reset hold on b was fixed

Ted – Wants to clarify if we are voting this figure in.

Carol – try to get to consensus on Fridays

Ted – There are some reasons this figure is not

Ted- email was misinterpreted and would like to clarify

Ted- thought that this was for a broader intent to bring up the device in a usable state and not just a reset. If it is just a reset block than no argument.

Carol – trying to keep it simple. Do allow some flexibility with C option user defined bits where you could put other information in the register.

Ted – suggesting that behavior of blocking resets needs to be more global and not specific to this register.

CJ- what does reset mean to you

TED – POR state

Ted – if we only block one register we are only a tenth of the way.

CJ – you do have the ability route resets

CJ – purpose of Clamp hold is to locally control the mode signal to the pins.

Ted – justification for block here was didn't want to force everyone to do clamp hold.. but it applies to all

Carl – you want this reset bit to block TLR globally?

Ted – want a test persistence that blocks that has nothing to do with Clamp Hold.

Carol – global TLR was a topic discussed on Friday but tabled because ted wasn't there.

Back to Reset-Select Register to let Carl finish

Lots of changes in Rules section. Reordered and rewritten

This is a stake in the ground for where we are now. Not definitive.

Carl reviews the changes made to the Rules section and goes through each rule.

Carol -- Should take "usually an input pin out of rule F

Ken – make a note after

Permissions

Description

Has been heavily rewritten
Group will review change off line

CJ takes control back and discusses Clamp Persistence

Carol – ted were your comments about IC reset or blocking test logic reset signals in a controlled

Ted – came up in context of IC reset. Point is to do it more globally and ic –reset because more simple.

CJ – IC RESET and RESET Select register

Didn't think as a group that we could globally say for every TDR that the signal should be blocked.

Clamp Hold is to hold pins to prevent mode signal so we can keep the pins in a test mode.

IC Reset needs its own blocking. Cost of ff we give capability to clear or not clear at reset.

With CP hold all the pins and will allow us to run on chip functions. But leave the pins clamped, needed to support in-sitчу abilities.

When you have ClampHold and on chip JTAG accessible function that needs pins and control locally. Still want control over some pins but leave others in test mode.

Ted – don't think we can merge the modes together globally. Where does requirement to hold pins during functional tests come from.

CJ – in sitchu test shows this

Ted – this isn't always the case.

CJ – leaves the decision to designer.

Ted – problem comes when you merge the 2 functions into one instruction, you have to implement both and don't have the ability to pick one.

Carl – never had to design a chip where all registers were reset by tlr.

Ted – any TDR that may interfere with functional behavior has to be reset by tlr.

CJ – what rule do we have that is hurting you

Ted – doesn't want to do clamp hold. But wants to be able to block TLR.

Ted – why not do it more globally.

CJ – don't have that capability. You can do something with reset select. Don't have a way to define it for all cases.

CJ reviewed Visio drawing of Clamp Persistence Controller.

CJ – need update state on Clamp Persistence Controller. Sees toggling during clamp hold.

Carol – addressing ability to clamp some pins while not clamping others.

We have a bunch of TDRs that we don't reset with TLR.

Consider debug TDRs a functional mode. And may have higher priority than mission mode.

Ted – if your registers don't respond to TLR, what difference does it matter if it is blocked

Carol – has consequences with other blocks.

KPP – Thinks that Ted’s way and CJ’s way can co exist with current method.

Depends on how you define instruction

Carol – put permission on Clamp Hold instruction so that it can be over ridden.

KPP – when I define my own instruction I can do what I want.

Adam C – does modification lead to automation or to do what you want (which doesn’t have a great value)

Carol – some automation.

CJ – this it is a good idea.

KPP – likes the idea of this being added as a permission as it gives guidance.

KPP – wants to change clamp persistence to test mode persistence because it is clearer.

Do we think we should change phrasing?

CJ – asks for thumps up/down for update register.

KPP – in principle it sounds like we need an update

CJ – is CH SYSRESET wrong with IC RESET?

Roland – concurs that there is some overlap with these instructions. Where Clamp Hold could control reset or IC RESET can control reset.

Carol – are you agreeing with extra bit in diagram?

Roland – just pointing out that there is a lot of overlap

CJ – what is the overlap.

Roland – SystemReset might now be an IC reset.

CJ – overlap is good. It is intended.

Carol moves to adjourn.

Seconded

Meeting adjourned: 12:10 EST.

Next Meeting: 2/1/2011 11:00 AM EST

NOTES:

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.

1. Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.

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8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.

Weekly 1149.1 Meeting coordinates

1. Please join my meeting.

<https://www1.gotomeeting.com/join/172495048>

United States: **+1 516 453 0012**

Meeting ID: **172-495-048**

Audio PIN: Shown after joining the meeting

2. Other call in numbers

Australia: +61 (0) 8 6365 4094

Canada: +1 416 800 9290

Germany: +49 (0) 898 7806 6462

Netherlands: +31 (0) 208 080 380

Sweden: +46 (0) 852 503 470

United Kingdom: +44 (0) 203 051 4835