IEEE 1149.1- 2011 Boundary Scan Working Group Minutes

Date – 02/08/2011

Attendees: CJ Clark, Bill Tuthill, Adam Cron, Craig Stephan, , Ken Parker, Carl Barnhart, Dave Dubberke, Wim Driessen, Brian Turmelle, Heiko Ehrenberg, Carol Pyron, Francisco Russi, Roland Latvala, Adam Ley, Mike Richetti, Bill Eklow,

Missing with pre-excuse

Missing: Lee Whetsel, Neil Jacobson, John Braden, Ted Eaton,

Agenda:

1. Patent Disclosure Slides
2. IC_RESET Wrap up
3. Clamp_HOLD
   a. Presentation/Proposal by Ted on rationale
   b. Do we understand the effects of blocking TLR to all TDRs in all ICs which may follow the standard?
      i. Additional burden for designers to make sure no damage can be done?
         1. "I was expecting that a TLR would happen…"
   c. Do we allow clamp to have both functional and test mode?
      i. Do we lose the benefit of CLAMP_HOLD that we seek by doing this?
      ii. Would private instructions or BLOCK_TLR instruction make more sense?
   d. What editorial work is impacted?
4. New Business

Meeting Called to order at 11:06 am EST
Minutes:

Review Patent Slide

CJ has sent out updated figure for IC RESET in email to add in OR gate and reordered mux
CJ asks to move to put figure in Draft.
No Objects made
Carol – Feedback from a designer to make sure that reset hold update state and reset enable and reset control gate into Boolean logic and system reset pin. As we transition from different states want to make sure that Boolean Logic can't glitch in permutations
CJ – suggests a rule.
Carol – figure should be illustrated so that it is glitchless. Enable and control should happen on different cycles. So only one thing is happening at a certain time.

Carl – Two OR's and AND gates have been replaced with a mux and makes it more robust.
Carol –a mux can still glitch.
KPP – need note to make mux glitch less
Carol – don't know what system reset pin is doing
Carol – not a rule per se but a caution or warning on diagram
CJ – note to say to set reset enable first.
      Even if glitch it will drive low and go to reset after glitch so might not be a problem.
CJ – all good input. Should add text to guide the designer.
CJ – do we want to get the IC RESET figure in draft?
KPP – no problem with figure
Francisco – would like to see some timing diagrams
      Concerned about glitch. Might want an example of implementation of logic
      Wants to make sure that all the signals are accounted for and no surprise in logic.
CJ –   Suggest Francisco to help make a timing diagram for figure.
Francisco will help Carl and work on timing diagram.
Carl – any objections to moving figure to draft from strawman?
No one objects.

Motion to incorporate IC RESET figure from strawman into draft
Motion passed unanimously. No one objected

Bill E- thinks there should be a way to allow
CJ - agrees
      Doesn't think the votes are there to change clamp hold as Ted was looking
Carol – question for Bill. Is the tool going in and out of test logic reset?
Bill E – For the most part Cisco doesn't go in and out of TLR.
      Ted's issue is based more on a system level perspective. Where the system is already started up.   Is the system resetting anything prior/during/after the BIST engine. Not something we any have direct control over.

CJ – Not the general practice the reset* signal is routed to all the TDRs and updates.
      Hard to find good examples where the reset* is routed to all the TDRs.
Carol – reset is OR'd in with TLR State at Freescale.

CJ – has a presentation for the group. Correlation between IC tester and IC in system.
      Difference between testing in ATE environment and in system environment
      Clamp Hold addresses Long scan-chains with incompatible pin modes for instruments.
      Clamp Hold may end up mandatory
         Test mode is not guaranteed to be functional any longer for any Private Instruction
         For any on chip to off chip IP local mode control is needed for your ip.
      "All my I/O are in functional mode"

Not something you want to happen. Cases where you would want to clamp some IO while running test on other IOs. Don't want all chips in functional mode.

Can't get into isolation without partitioning

With partitioning we get JTAG being a superior method to access portions of a chip

KPP – agrees with CJ's last slide. Shows why something needs to be clamped and other pins left alone

Carl – Ted's points rebut what was in CJ slides and Ted should have an opportunity to make points against the slides. Sees counter points

CJ – this is what makes partitioning so powerful

Carl – needs to be some way of eliminating the TLR at the wrong time.

CJ – that is what we are addressing 1687 and we should do it as well because it makes sense.

Carl – need to create new rules that say TLR is not a parking state.

Bill E – we would be concerned if there was a universal mandatory use case.

CJ – don't have to load Clamp Hold and can run functional IP.

Bill E – concerned seeing slide saying Clamp Hold would be a mandatory instruction

CJ – would have instruction but don't need to use it.

Bill E – so we would have to support the ClampHold instruction in Tap controller but don't have to use it?

CJ – Correct.

CJ – will send out slide set.

Mike – doesn't reset any TDRs with TLR

CJ – don't need to use TLR to set conditions of flop.. Can use a POR.

Meeting adjourned: 12:05 EST.

Next Meeting: 2/15/2011 11:00 AM EST

NOTES:

Current Issues listed and who will champion that issue.
1   Observe only. –   Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.

8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:
*   CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
*   Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
*   Comment #8 CJ will make changes to draft for observe only
*   Comment #7 CJ will get in touch with Doug to get input regarding Comments
*   Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
*   Comment #4 Adam L to add comment about TRST. Update figure 6.8
*   Comment #3 Adam L will update language for any proposed change for this section.