IEEE 1149.1- 2011 Boundary Scan Working Group Minutes

Date – 03/22/2011

Attendees: CJ Clark, Bill Tuthill, Adam Ley, Carl Barnhart, Carol Pyron, Roland Latvala, Brian Turmelle, John Braden, Dave Dubberke, Francisco Russi, Ted Cleggett, Wim Driessen, Ted Eaton, Ken Parker, Heiko Ehrenberg, Craig Stephan,

Missing with pre-excuse Adam Cron, Mike Richetti, Bill Eklow,

Missing: Lee Whetsel, Neil Jacobson,

Agenda:

1. Patent Slides and Rules of Etiquette
2. Clause 8.19 and 8.20
3. PDL Annex C   - Review Discussion

Meeting Called to order at 11:04 am EST
Minutes:

Review Patent Slide

Carl: Non invasive instructions always have a rule that says that the test logic shall not interfere with IO pins and system logic.
        IC RESET function will persists after IC RESET goes away. So there is interference on functional reset pins so rule c) was changed
Ted: isn't reset going to change the behavior of IO
Carl: original Rule c) test logic can't interfere with functional logic so addition of reset description added.
Note after c) to add clarity about system level response to reset
Carl: rule change will have to be added to the other non invasive instructions.
Carl: requests that clauses 9 and 10 be reviewed for this week and prepared for next Tuesday.

Carl moves to accept changes to date for 8.19 and 8.20 without prejudice to changes at a later date
        Ken Seconds
        Discussion:
        Note after c) will be a change after the adoption. . This will still show as a change.
        Carl will insert 8.20.1 later
        Non Opposed.
        Motion passed.

Clause 9
General test data register clause

Recommendation to have design specific test data registers be accessed by a single instruction in order that they can be used with PDL.

Francisco: Is PDL a reserved word

CJ: No this isn't a reserved word. Not in the BSDL

Carl: will add PDL to the glossary

Carl: Figure 9-1 was updated

9.2 has new information and should be reviewed

9.3 No changes.

Carl and Carol discuss the symbology that is used in the draft

Ken: suggests not changing older figure symbols to match newer drawings

CJ: agrees with this

CJ: Points out that on these drawings in 9-3, the industry has moved from the gated tck to non gated TCK. Need to update tap controller figures to match.

Carl : gated tck is still used in boundary registers.

CJ: it is shown that way but not required.
        Need a volunteer to update figure 6-5 to remove gated clock.

Carol: what is the opposition to gated clocks

Ted: both are prevalent. Sees it going both ways.

Carol : industry knows how to move to a gated clock and back.

CJ: should be showing both ways in figure 6-5

Carl will update the figure to show a non gated clock path

Section 10 does not have big changes

Review of Annex C

Figure C-1 added - use mode of PDL

CJ still needs to present to the 1687 group the changes that 1149.1 needs to PDL. Doesn't expect any issues with the 2 groups being able to be in sync.

Carl: why is iPDLLevel an action and not setup? Should it be a compliance

CJ: Action that the tool will figure out what they are doing. Maybe more compliance

Cj: no concept of PORT and allows registers to be remapped.

CJ: Roland had suggested iREAD be called iExpected. It is not really reading but setting expected data.

Ted: it is doing more than that. Telling the tool when getting an iAPPLY to do the read. Makes the scan happen

Carl: it is not storing the data

CJ: will be some differences between 1687

Ted: not making a substantial difference. We should stick with 1687's PDL unless we are making a big impact

Ted: in PDL level 0 there is no way to do anything with the data coming back so there is no reason to return the data.

CJ: in our environment of PDL level 0 we are only using the iREAD command to do a compare of data with expected and actual.

Added –IR to iAPPLY. Need to transverse the IR path

Carol: does the word "instruction" need to be a reserved word. May show up more than once.
CJ: Hierarchy can handle the duplicates
Carol: wants a list of key words for PDL

CJ : added section about reserved PROCs
      Added idea of "main"

Meeting adjourned: 12:03 EST.

Next Meeting: 3/22/2011 11:00 AM EST

Motions Made and Seconded
Motion to accept changes to date for 8.19 and 8.20 without prejudice to changes at a later date
      Passed unopposed

NOTES:

New Teleconference information. Now using Live Meeting.

Join the meeting

Meeting time: Tuesdays 11:00 AM (EST)   (Recurring)

AUDIO INFORMATION
-Computer Audio(Recommended)
To use computer audio, you need speakers and microphone, or a headset.
-Telephone conferencing
 Use the information below to connect:
      Toll: +1 (218) 862-1526
      Participant code: 11491

FIRST-TIME USERS
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Unable to join the meeting? Follow these steps:
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      Meeting ID: F9R6S6
      Entry Code: k/d6<@M6j
      Location: https://www.livemeeting.com/cc/intellitech
If you still cannot enter the meeting, contact support.

Current Issues listed and who will champion that issue.
1   Observe only. –   Ken and Carl
1.   Directionality linkage. - CJ
2.   Power Pins. - Heiko
3.   Pairing power pins with functional I/O - CJ
4.   Sample / Capture. – Carol (Freescale) & Roland
5.   TRST included in PCB level diagram. – Adam L.
6.   Slow to Fall/Rise signaling issue – CJ
7.   "No Connect" – Ken and Francisco.
8.   Device ID – Still needs work
9.   Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:
- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.