

**Date – 03/29/2011**

**Attendees:** CJ Clark, Bill Tuthill, Brian Turmelle, Carl Barnhart, Carol Pyron, Wim Driessen, Adam Ley, Heiko Ehrenberg, , Bill Eklow, , Ken Parker, Dave Dubberke, Ted Eaton, Craig Stephan, Ted Cleggett,

**Missing with pre-excuse** Roland Latvala, Adam Cron, Francisco Russi, Mike Richetti

**Missing:** Lee Whetsel, Neil Jacobson, John Braden,

**Agenda:**

- 1) Patent Slides and Rules of Etiquette
- 2) Clause 13, 14, 15 discussion
  - a. *Discussion 14.1.1*
- 3) PDL Annex C - Review Discussion

**Meeting Called to order at 11:05 am EST**

**Minutes:**

Review Patent Slide – Reminder sent out over email during the last week.  
Review of Working Group Meeting Guidelines

Clause 13 The Init Data Register

13.1 Carl edited section adding in comments from email discussion over week  
Carl thinks that 13.1.1 b) should be a rule and not a recommendation

Reason not to have b) as a rule would be difficult to do.

CJ: If rule it would be saying that the value would not be changed by the assertion of TLR/TRESET.

CJ: If it is not a rule you have to create a rule to say that init run has to follow init-setup so you don't lose any data

Carol : objection is requiring an update state.

CJ: doesn't say it requires an update state

Carl: should be persistence across anything.. init data only be modified by re-execution of init-setup

Ken: who controls the multiplexor and when

Carol: if the active instruction is EXTEST, CLAMP , or HIGH Z

Ted: in his world that mux is controlled by a TDR bit. Cleared by TLR/Treset

Carol: if it was a rule you couldn't make it a bit in the init-data

Carl: if it was a black box no one would care

Ted : as a general rule the register should respond to Treset or TLR. Should not be cleared by system logic.

Trst and TLR are not the same thing in this version of the standard.

CJ: focus on that we don't have additional rules that go with b). Nothing that prevents data from being cleared if b) stays as a recommendation

Ted: why wouldn't I expect for everything to clear if we are not in Test Persistence mode.

Carol: need to look at all the cases with Test Persistence and make sure it is clearly defined. Agrees that we should take this offline

CJ: should break up b) to cover all the cases so not everything is in this recommendation

Clause 14 Init Status Register

Optional Register

Carl: Rule that it needs to be dedicated test register.. Why?

d) Is the minimum length this a rule or a recommendation?

CJ: 14.1.1 b) Why can't it be a shared register?

Ted: thinks it can be shared.

CJ: people who object to having it shared

Ken: doesn't object but doesn't understand the implications. So does not want it

CJ: What would you be sharing it with if you did share it?

Carol: might want to share with high pin parts.

Carl: not sure anyone would want. Bypass register isn't dedicated test logic.. Shareable in theory.. if no reason to dedicated there isn't a rule.

Carl: anyone object to removing rule b)

CJ objects. Doesn't fully understand the implications. Would error on the side of caution

Ken: low cost safety value so leave it.

Ted: is ok the way it is

Carl: is d) a recommendation or a rule

Ken: would like to see d) be a rule

CJ: INIT-SETUP and INIT-RUN are departing a little bit from 1149.1 vision. Here we will have side files to configure complex IC. Lack of visibility into initialization process is a concern for CJ. No observation into how the processes completed(failed)

Ted: doesn't care about the number of bits in init run if init setup and init run are paired. Why does it need to be 2 bits to give status?

Carl: Done bit was one that Ted wanted to do polling. (Finished)

Just having a pass bit would have polling go on indefinitely

Ted: Agrees with that but shoehorning all the different done and pass bits into these 2 would not be practical.

CJ: concerned to have a 5 bit register used for initializing something and there will be illegal combinations. Illegal combinations would give a fail indication

Ted: great case but only one case.

Ken: Should be a concept of a done. 2<sup>nd</sup> bit can be copy of first if circuit is so simple that there isn't a pass/fail indication

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Ted: doesn't want to present false information to the end user

CJ: would like to give the ability to display if there was a pass or fail. Can use info field in BSDL to indication that the pass/fail status bit was not used.

Carol: agrees with CJ. Need to consider different types of IC design.

Ted: is for recommendation. Not forcing anything. No objection either way. Only wants init-run to be optional. Otherwise doesn't care.

Carl: would it make a difference if on d) 2 – to add phrase "if such information is available" and allow it to be a duplicate of bit 0 if there was no information

CJ: not for it

Ken: make bit 0 a rule. Make bit 1 a recommendation. And bit 2-x is test information.

Carol: likes this approach

CJ: will have to think about it.

Carl: will expand d) bit 0. This will be a "shall". Bit 1 recommendation. Along the lines of what Ken was saying. And then send out to the group for review

CJ: would like to define bits better. Is there a way to capture illegal states?

Carl: mnemonics

CJ: doesn't like to read back a 1 bit (single bit) status.

Carol: in optional bits you can have a signature to prove that you had shifted correctly.

CJ: would like to have breadcrumb bits so you know you are talking to the thing you think you are talking to.

Carl: do we want this on InitData?

CJ: something we should think about.

Carl moves to adjourn

Seconded

**Meeting adjourned: 12:05 EST.**

**Next Meeting:** 4/5/2011 11:00 AM EST

No Motions Made

NOTES:

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Meeting time: Tuesdays 11:00 AM (EST) (Recurring)

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### Current Issues listed and who will champion that issue.

1. Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

### Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8

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- Comment #3 Adam L will update language for any proposed change for this section.