Date - 07/12/2011

Attendees: CJ Clark, Bill Tuthill, Craig Stephan, Adam Ley, Roland Latvala, Francisco Russi, Carol Pyron, Wim Driessen, Dave Dubberke, Brian Turmelle, Heiko Ehrenberg, Josh Ferry, Carl Barnhart, Ted Eaton,

Missing with pre-excuse Ken Parker,

Missing: Lee Whetsel, Neil Jacobson, Mike Richetti, Ted Cleggett, Matthias Kamm Peter Elias, John Braden, Bill Eklow, Adam Cron,

Agenda:

- 1) 11:00 Patent Slides and Rules of Etiquette
- 2) 11:05 Draft Discussion
 - a. B.8.18
 - b. Register_Assembly
- 3) Homework assignments

Meeting Called to order at 11:00 am EST Minutes:

Review Patent Slide – Reminder sent out over email during the last week.

Review of Working Group Meeting Guidelines

Review B.8.18.1

Wim – iwrite/iread/safe/itrst/etc assignments. Why are these key words being used to describe a register rather than the cell of the registers.

CJ- different than BSDL boundary register portion. Here we have internal TDR and to assign a mnemonic to a single bit wouldn't have the meaning that we are looking for.

Looking at these as a quantity of bits which have more value

Wim – example- IREAD description on 7664 is confusing. Description sounds like a cell.

Carl – thinks the name should be changed. IRST could be TLRST. IREAD could be something with CAP. Get rid of the confusing I nomenclature

Ted – agrees with Carl.

Carl - feels the names no longer work

Adam L – reuse word "capture"

Carol – get rid of i words

Group will leave it up to Carl to update the keywords.

Francisco – why did we use i in the keywords

Carl – borrowed from PDL (1687) when working on the init data

Francisco – are we changing PDL

CJ – no.. only changing in BSDL to clear up any confusions.

IEEE 1149.1- 2011 Boundary Scan Working Group Minutes

No motion made to change keywords.

Carl points out that the current method of this group is to come to agreement and then vote on the sections in the draft

Carl feels that the current method agreement in the group is working and no need to change it.

Draft update

Carl feels that the cleanup will take until the end of August

Keeping examples in the standard based on registers in the standard

CJ – feels that extra examples will help people understand some of the things that they can do

Carl – feels with the SERDES and init data examples has enough material

CJ – what about the MEMD examples, will that get deleted

Carl – perhaps they will get deleted, will go back and look at it.

Ted – wants to know about discussion from Friday, on if all these pieces are needed in 1149.1

Carl – wants to get things documented and then let people decide if it is needed

Ted – doesn't want things to get left in because the work was done and by default it stats.

Carl – we as a group will go through information and then vote.

Group moves to completing a discussion started on Friday's meeting. It was brought up that too much complexity is being added to the 1149.1 standard

Ted – Fridays' meeting brought up some questions of complexity in dot 1 CJ had missed Friday's meeting due to travel

Carl's summary of the meeting was - Do we as a working group feel that it is appropriate to include features in the BSDL that are intended to make the debug process easier or just support reading and writing the registers . is it appropriate to specify the way debug is done?

Ted – there is already a standard that is in the works based on 1149.1 that provides this debug capability and more so why are duplicating the work being done in group here in 1149.1 (*standard that Ted is referring to is p1687*)

CJ – depends on how you define debug. Features are not necessarily for debug. In order to run a test through a SERDES to do a PRBS we need to be able to setup the interface to make the test work. Agreed that you don't need it during production but need to get the interface working to get to the patterns needed for production.

1687 was never brought as a standard that would close and limit 1149.1

Feels that there is great utility in 1687 but what we are doing here in 1149.1 will help the base of the industry keep going.

Ted – Feels that this added complexity is only for running instruments inside chips.

Which is what 1687 does. From Fridays' meeting it was clear that many people felt we were going too far

Carl – there was only a fear of it

Carol polls the group to get their opinion

Josh – doesn't see anything wrong with extensions. Sees overlaps in other things (computer languages). feels that the IC developers gets different methods to describe

registers. Simpler can use 1149.1. more complex you can use 1687. The BSDLs could grow out of proportion but that would be different problems. Can't tell what the world will look like 10 years.

Adam L – to some degree there are some concerns in this area that perhaps the understanding of the appropriate domain of the 2 standard is not as well understood as it could be and some overlap could occur.

Carl – would it help to have the full examples to see what we are proposing?

Adam l – can't say that wouldn't' hurt. But that is the nature of the concern, perhaps the effort here better invested there or visa versa.

Francisco – doesn't see any problem with the progression from init data to these registers.

Bill T- doesn't see any problems with the overlap. Feels that the two standards can coexist

Wim – concerned about the functional information might be leaked out

Carl – doesn't see a problem where the functional information of the registers would get leaked out

Wim – can't provide an example right now but that is his concern

Carol – some of the complexity was added to standardize IO configuration for FPGA May seem more overlap than expected but doesn't' see a problem.

Should be concerned about what other people in the industry think

Roland – private instructions done for years. So these are features not a problem. On the right track.

Ted – when ken brought up his problems on Friday they were unrelated from 1687, Ted's additional comment was that we can accomplish these things in 1687 and don't have to be in 1149.1

Carl – bring this up again when there is enough done in the draft so that we can argue from real stuff.

Carol – good point and no problem revisiting in the future

CJ – had discussion about complexity, John B had brought up the good point that the complexity of the IC's are already there. This will ripple down to complexity to the BSDL.

Homework assignments.

Heiko and Carol's assignments are outstanding and will be done for next week's meeting

Bill E – work on more concrete example and definition of the ESSID register

• Meeting adjourned: 12:07 EST.

Next Meeting: 7/19/2011 11:00 AM EST

0 Motions Made

NOTES:

1149.1 working group website - http://grouper.ieee.org/groups/1149/1/

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Meeting time: Tuesdays 11:00 AM (EST) (Recurring)

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