IEEE 1149.1- 2011 Boundary Scan Working Group Minutes

Date – 08/16/2011

Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Adam Cron, Wim Driessen, Craig Stephan, Roland Latvala, Roger Sowada, Adam Ley, Carol Pyron, Carl Barnhart, Dave Dubberke, Ken Parker, Heiko Ehrenberg, John Braden, Francisco Russi,

Missing with pre-excuse

Missing: Lee Whetsel, Neil Jacobson, Mike Richetti, Ted Cleggett, Matthias Kamm , Peter Elias, Dharma Konda, Josh Ferry, John Seibold, Ted Eaton, Bill Eklow,

Agenda:

- Patent Slides and Rules of Etiquette
- B.8.3
  - **Motion Needed: Motion to accept B.8.3 Logical Port Description as presented in PDF on the reflector subject to any wording improvements**
  - Attribute POWER_PORT_ASSOCIATION
  - **Motion Needed: Motion to include attribute POWER_PORT_ASSOCIATION as presented in updated form on Friday 8/12 2:18 on reflector subject to any wording improvements**
- B.8.7.2 c
  - c) All non-linkage and non-power ports in the <logical port description> of a given BSDL description shall be referenced in each <pin mapping> of that description, and vice versa.
  - **Motion Needed: Motion to change the rule to include all ports as follows:**
  - c) All ports in the <logical port description> of a given BSDL description shall be referenced in each <pin mapping> of that description, and vice versa.
- B.8.14.3.8 <input spec>
  - **Motion Needed: Motion to accept B.8.14.3.8 in current draft subject to any wording improvements**
- Further discussion on mixed R_F/R_A
- Homework assignments

Meeting Called to order at 11:07 am EST
Minutes:

Review Patent Slide – Reminder sent out over email.
Review of Working Group Meeting Guidelines

B8.3 Logical Port Description
Section 8.3.1
Carol – did we result that “No connects are Linkage Mechanical”?
Ken – no
CJ – the only place you have no connects are in the PinMap

Carol – does anything in the pin map need to be in the PortMap
CJ- the pinmap is not optional. What is option is including the non boundary scan pins in the pin map

The rule is that we currently allow Linkage pins for instance not to be in the pinmap. This doesn't make sense.
Carol – this is the 2001 state?
CJ – correct
CJ – this is a different rule however than what we are on - 8.3

Carl – non boundary scan you are still allowing ROO on those pins such as a VREF in? But these could be boundary scan?
CJ – yes there could be tweaks.
Adam C – are we getting rid of "Linkage" all together or is there an option to leave "Linkage" in
CJ – no.. There would be no way to get anyone to do this if we still allow "Linkage"
Carol – want to get people to direct the pin to the correct category
Carol – "no connects" are these Linkage Mechanicals.
CJ – no. they would be what ever description best suits the pin from the list. "No Connects" are not a port description.. They are in the pinmap
CJ – going to declare them to whatever these "No Connects" are
Francisco – still have linkage coupled with No Connect. Need to decouple linkage from no Connect
Carl- "no connect" says we have a port on the silicon and there isn't a pin on the package that we are putting the silicon into.
Cj – what we are describing is the Silicon. Either have an electrical port or non electrical port. if it is electrical than use a port description. If it is non-electrical in nature it is linkage mechanical. If it is not connected in the pinmap you need to use the *
Carl- should drop linkage mechanical as there is nothing in the silicon to match
Adam L – linkage mechanical is like an * in this domain
CJ – we have mechanical balls that are present in the pinmap and linkage mechanical provides a place holder/map to get to the port list.
Carol – everything that is the pinmap will be in the port list?
Carl – yes that is correct
Ken – table B.2 should describe Linkage Mechanical better
Carol – agrees
Carl – if we adopt it we will add to it

CJ – Symantec checks already occur in 2001 to check boundary cells. You cannot have a boundary scan cell on linkage.
Carl – moves to **adopt the basic constructs of B8.3.1 subject to future editorial changes.**

Heiko Seconds

Carl – idea of no connect is that you port on the silicon where there is no package pin if you have a package pin that is not connected on the board there is way to describe in BSDL.
Roland – if the die isn't bounded to the silicon

Carl – it can be defined as the function of the pin on the silicon
Ken – opposite case is the question.
Roland- * is that there is no pin?
Carl – yes.. no pin or ball on package.
Carol – port on silicon that does not have a ball do you document that and does it have a boundary register?
Carl – whether you have a boundary register is independent of the package you are putting it in.
CJ – there probably are cases of odd things where it requires 2 BSDLs if you are to change the package.
Carol – when we have 2 packages parts (big and small) there is a package select IO on the silicon that is tied in the package that tells us which package the silicon is.
Carl – I think this is a pinmap question and can we put that on hold.
Francisco – Carol should be able to make here point as it is still part of linkage.
Carl – linkage and no connect are independent
Cj – still getting confused between the pin map and the logical port section.
Only voting on the Logical Port Section
No connect is a package construct.
Ken – believes that Carl has enough information and calls the question

adopt the basic constructs of B8.3.1 subject to future editorial changes
12 yes - CJ Clark, Bill Tuthill, Brian Turmelle, Wim Driessen, Craig Stephan, Roger Sowada, Carol Pyron, Carl Barnhart, Dave Dubberke, Ken Parker, Heiko Ehrenberg, John Braden, Francisco Russi,
1 no – Adam Ley
2 abs - Adam Cron, Roland Latvala,
Motion passes

Attribute Power Port Assocation
Ken – question about Vref
CJ – from Vref association to PowerPort association
CJ – so left of the colon can be a power or Vref_in association
Adam C- a Vref can only go to a pin but a power can go to the same pin?
Carol – they have to?
Carl – the names on the right of the colon can be duplicated for multiple names on the left.
Carol – and the power port association key word is option and not mandatory
CJ – correct
Ken – what is the position of this station in BSDL
CJ- undefined
Carl- probably after the port association
CJ – probably should be something towards the end where the other new associations are located.
Needs to be after the port.
Seems cumbersome to stick it at the top
Carol – would like to use bus notation (list a bit vector)

CJ – would work in other section but not here. Really going to 1 bit to many
Carol – uses buses. Doesn't see it as only 1 bit
Would like the bit vector
CJ – what we are after today is to include an attribute called PowerPort association. Need to add the attribute before we can describe the rules
Carol – makes motion **to include an Optional Attribute called Power_Port_Assocation**
Carl - suggests modification
To move forward with Optional attribute Power_Port_Assocation with details subject to modification by working group
Brian Seconds
Ken calls the question
Motion passes
14 Yes - CJ Clark, Bill Tuthill, Brian Turmelle, Wim Driessen, Craig Stephan, Roland Latvala, Roger Sowada, Carol Pyron, Carl Barnhart, Dave Dubberke, Ken Parker, Heiko Ehrenberg, John Braden, Francisco Russi, Adam Cron,
1 No- Adam Ley,
0 Abstain

B8.7.2.c
In 2001 the rule is non-linkage and power ports listed in the port list should be listed in the pin map
This rule makes the
CJ – Why wouldn't we have all the ports in the pinmapping
Carl – objection from past experience is that power and ground pins are ½ the number of pins on a BGA package and doesn't add much value to the test process. You are not including those pins in boundary scan tests
Would have to at least extend the definition to any port that is included in the boundary scan register because of the ROO we can have Vrefs in the boundary scan register.
Cj – Some objection to its not usefulness have shown that power pins are important to generate board tests.
Carl – straight VDD and VSS basic core logic. Not sure what value listing those have.
Doesn't see where the information on the bulk power does you any good.
Adam C- you get close with board level netlist, you don't need to know at the bsdl level if they are power and ground because you get that in the netlist?
CJ – only if the information is there. Not all power pins are put in the netlist or always clear
Carol – Carl's comment was on the bulk power pins VDD VSS. Are you saying that is important to figure out?
Wim- Helps when analyzing board it is important to know where the power and grounds are. Good to be in the model
Heiko – as a tool vendor I would want all the physical pins listed in the pin maps.
Roger – easy to put it all in the pinmap. Whatever makes it easiest for the tool vendors.
CJ – it's always a guess if it you found it in the pin map. Not sure if it if an error or not.
Roger- have caught mistakes in the past so he agrees

Carol – have documented every pin in the package in the pinmap. So we can make sure you have them all. Not opposed to putting it all in there.

HomeWork Status

John has passed his examples in to the working group. CJ is running them through the parser.

Carol – is still working on examples
Heiko is still working on examples.
CJ is still working on port assignments

Homework assignments.

Heiko and Carol's assignments are outstanding and will be done for next week's meeting

CJ will have examples of port assignments
Bill E – work on more concrete example and definition of the ESSID register

- **Meeting adjourned: 12:04** EST.

Next Meeting: 8/23/2011 11:00 AM EST

2 Motions Made

1. **adopt the basic constructs of B8.3.1 subject to future editorial changes**
   a. **Motion Passed**
2. **To move forward with Optional attribute Power_Port_Assocation with details subject to modification by working group**
   a. **Motion Passed**

NOTES:

1149.1 working group website - http://grouper.ieee.org/groups/1149/1/

Now using LiveMeeting as audio/video conference software

JOIN the meeting as PRESENTER - this way you will not need to be made a presenter

Just one person needs to connect VOIP to phone system. It's usually me, but if you connect first, you can connect the VOIP to the dial-in with the sequence below. Within LiveMeeting you must connect the Audio to enable the Conference calls. (Just we don't want to do it more than once).

Voice and Video -> Options -> Connect Telephone and Computer Audio -> Dialing Keys

ppppp11491p*pp03820#

JOIN the meeting as GUEST – will have to ask to present

Meeting time: Tuesdays 11:00 AM (EST) (Recurring)

AUDIO INFORMATION

-Computer Audio(Recommended)
To use computer audio, you need speakers and microphone, or a headset.
-Telephone conferencing
Use the information below to connect:
Toll: +1 (218) 862-1526
Participant code: 11491

FIRST-TIME USERS

To save time before the meeting, check your system to make sure it is ready to use Office Live Meeting.

TROUBLESHOOTING

Unable to join the meeting? Follow these steps:

1. Copy this address and paste it into your web browser:
   https://www.livemeeting.com/cc/intellitech/join
2. Copy and paste the required information:
   Meeting ID: F9R6S6
   Entry Code: k/d6<@M6j
   Location: https://www.livemeeting.com/cc/intellitech

If you still cannot enter the meeting, contact support.

NOTICE

Microsoft Office Live Meeting can be used to record meetings. By participating in this meeting, you agree that your communications may be monitored or recorded at any time during the meeting.