Date - 10/04/2011

Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Adam Cron, Carl Barnhart, Carol Pyron, Ken Parker, Dave Dubberke, John Seibold, Bill Bruce, Roger Sowada, Josh Ferry, Wim Driessen, John Braden, Francisco Russi, Roland Latvala, Dharma Konda, Bill Eklow, Jeff Halnon*, Sankaran Menon*, Craig Stephan,

Missing with pre-excuse Adam Ley,

Missing: Lee Whetsel, Neil Jacobson, Mike Richetti, Ted Cleggett, Matthias Kamm, Ted Eaton, Heiko Ehrenberg, Peter Elias, **Agenda**:

- 1. 11:00 Patent Slides and Rules of Etiquette
- 2. Review of SelfMon and Pulsemon cells
 - a. Looking for BSDL token
 - b. <type assignment>::= NOPI | NOPO | NOUPD | SELFMON | PULSEMON | <user type keyword>
 - Little change for the tool reader of BSDL. A method for IP providers, PDL writers to communicate the capability of the cell. Both cells add testability and PULSEMON reduces scans and enables an edge after UPDATED
- 3. PowerMUX
- 4. Enables INIT_DATA to traverse multiple power domains
 - a. Controls and senses power before mux is on
 - b. Mux enable allows scanning through power domain
 - i. Can this be used with boundary register?
 - c. PDL Level 1
 - d. mixed R F/R A
 - e. Homework assignments

Meeting Called to order at 11:10 am EST Minutes:

(meeting was off to a late start due to some Live Meeting difficulties)

Review Patent Slide – Reminder sent out over email.

Solicited input from anybody who is aware of patents that might read on our standard.

No responses.

Review of Working Group Meeting Guidelines

Ken and Bill Bruce will look into Multiple Device ID

Two new members - Jeff Halnon and Sankaran Menon

SelfMon and PulseMon

Carol: PulseMon, you could have a pulse generating cell without self monitoring. Should we have that in the standard? Can we make the monitoring part optional?

CJ: two cells. Pulse and PulseMon?

Bill B: Will these figures for PulseMon get referenced?

CJ: yes. They are described in the Cell

Bill B: would like some more description to the figures.

CJ: the editor will be tasked with that.

Carl: noted that changes are needed and will add labels

Francisco: This is already being tested in 1149.6. Are we overlapping?

CJ: no. It is not an overlap. we need to configure whether it is ac coupled or not

Carol: Freescale has basic init-setup ability and still have .6 support in chips

CJ: can you tell me more about what you are doing?

Carol: we have a few bits which select which protocol is needed and based on protocol selection it controls multiple selections to the driver.

CJ: if I had pre-emphasis is that another setting

Carol: yes it would be in that case

Adam C: are we showing too much.. Wanted an example of a register and some PDL. Can you show a cloud? Are our problems with the figure is that we have too much information.. Can we minimize it to get the point out

CJ: we can in the draft. But trying to work out the problem.

Adam C: under the impression that Init-data and Init-setup was some PDL that would get you to setup the device the way you want. Ignorance is bliss.

CJ: no there isn't a PDL that you can get and run. So the Bits do matter and description of the bits matter. The question is do we limit Init-setup to one scan or do we allow multiple scans.

CJ is concerned that SERDES IP is not being appropriately setup in a single scan and may need multiple scans to be setup

Carl: now that we have PDL for the side file, it can do multiple scans of the init register. Everything gets update at the same time across the board is important

If you have a sequential problem initializing your chip you will need a built in statemachine to do it. InitRun might not be sufficient because the IOs can change at any given time while Init Run is loaded.

CJ: is concerned the burden of the amount of registers to run a statemachine to setup the SERDES

Carl: that is a board problem that they have to deal with today

CJ: disagrees. Registered interface can be written to by mission mode logic so it can set the address and not use a statemachine. To do what we need, you would need to have a statemachine built in to load the data

Carl: agrees we shouldn't make an overly burdensome requirement. But there are ways to do it.

CJ: Thinks we should work out some of these more complex situations.

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Ken: a new layer of complexity that needs to be justified. But if the IC designers need it we can look at but if it was is taken care of today than we should see why it would be justified.

CJ: a lot of work to run the statemachine and write data into each parameter

Ken: this is why we have Init-Run

Carol: agrees that it is a lot of work but feels that there are many ways vendors can do this, but will want to minimize the use of this.

Roland: some manufactures may want to take the whole set of functional flops and put them on a TDR clock and use those mission flops in the scan chain.

CJ: wants to know how does the scan insertion tool identify the functional flops versus internal logic? Do we end up with internal logic in the scan chain.

Seems like more work and more burden to do this.

Want to move ahead with PulseMon? Should we take another shot to move toward the draft with a better figure?

Discussion will continue on email with possible motion made in beginning of next meeting.

• Meeting adjourned: 12:21 EST.

Next Meeting: 10/11/2011 11:00 AM EST

0 Motions Made

HomeWork Status

John has passed his examples in to the working group. CJ is running them through the parser.

Carol – is still working on examples

Heiko is still working on examples.

CJ is still working on port assignments

Homework assignments.

Heiko and Carol's assignments are outstanding and will be done for next week's meeting

CJ will have examples of port assignments

Bill E – work on more concrete example and definition of the ESSID register

NOTES:

1149.1 working group website - http://grouper.ieee.org/groups/1149/1/

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JOIN the meeting as GUEST – will have to ask to present

Meeting time: Tuesdays 11:00 AM (EST) (Recurring)

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