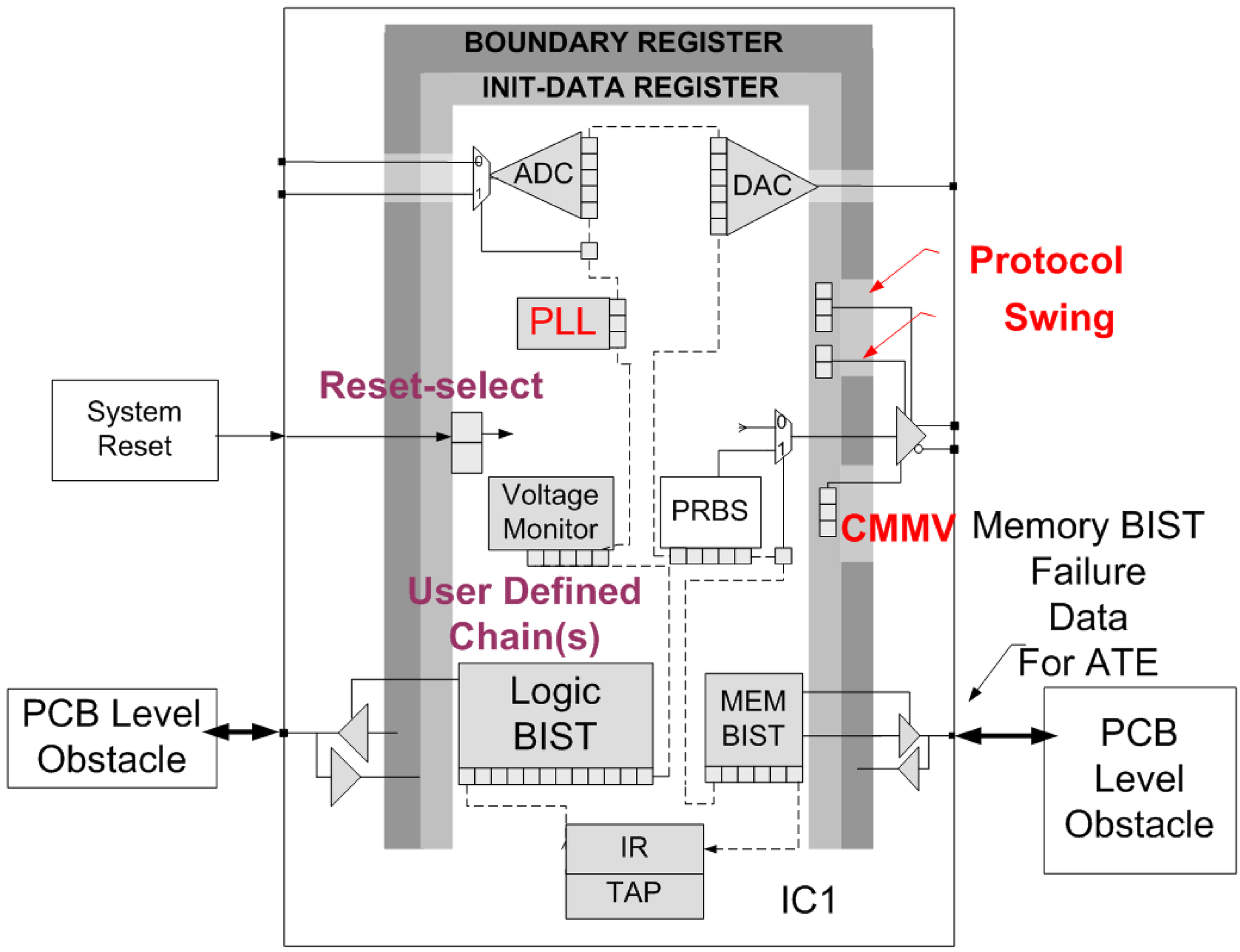
IEEE P1149.1-2011 UPDATE



New Instructions:

INIT_SETUP/INIT_RUN

- configure on-chip I/O & resources for test

CLAMP_HOLD/CLAMP_RELEASE

- hold pins & isolate for in-situ on-chip tests

IC_RESET – Reset isolation and control

- Reset of IC or domains through JTAG

BSDL attributes for Internal JTAG TDR registers

- for BIST/PLLs/SERDES IP blocks

MNEMONICS for JTAG register values

- Easy to remember words – start/stop, on/off

Package files for on-chip IP blocks

- self-contained definitions from IP providers

PDL Script files for device initialization/access

- Read/write registers via Mnemonics

Mnemonics and register sub-fields Guide user through GUIs

PROTOCOL1(10)	OFF	0000000000	0000000000
PROTOCOL2(10)	OFF SRIO PCIE XAUI	0000100000	0000100000
SWING(2)		00	00
PLL(2)		10	10
CAMBIST(2)	STOP	00	00
CAMSTATUS(2)	00	10	10
LBIST(2)	RUN	00	00
LBISTSTATUS(1)	0	PASS	PASS
MODESTATUS(1)	0	0	X
STATUS1(1)	0	PASS	PASS

IP level PDL can be re-targeted to IC

```
# run some basic tests on registers
iScope U1
iWrite LBIST RUN      # bit-position independent registers
iApply
iRunLoop 300000
iRead  LBISTSTATUS PASS  # check that LBIST passed
  iApply
  iWrite SWING S400MV     # set differential Swing to 400mv
  iWrite PROTOCOL1 SRIO   # set protocol to SRIO
  iApply
  iWrite CAMBIST RUN      # execute CAM BIST
  iApply
  iRead  CAMSTATUS DONE
```

New BSDL attributes support user TDRs

```
attribute REGISTER_FIELDS of Example : entity is
"init_data [505]  ( "&
"(Clock[5]      IS (504 DOWNTO 500) DEFAULT(Clockset(100Mhz)) ),"&
"(Protocol[3]   IS (302 DOWNTO 300) DEFAULT(Protocol(off))    ),"&
"(Voltage[2]    IS (101 DOWNTO 100) ), "&
"(Reserved[20] IS ( 19 DOWNTO 0)  )), " &
"myTDR[129] ( "&
"(Address[64] IS  (163 DOWNTO 100) ), "&
"(Data[64]    IS  (227 DOWNTO 164) ), "&
"(WE[1]       IS  (228)            ));"
```

New Files for IP Packages

```
package SerdesH is
use std_1149_1_2011.all;

  attribute REGISTER_MNEMONICS of SerdesH : entity is
   "BSTERM  (Norm       (100) <Normal RX Term. RX threshold @800mV >, " &
   "         Dis        (111)  <Termination disabled >, "&
   "         rsvrd      (Others) <Reserved - Undefined behavior>), " &
   "BSCM    (Norm_cm    (1)  <Normal TX Boundary Scan Common Mode>,  " &
   "         Diag_cm    (0)  <Diagnostic mode.  Low TX common mode>), " &
   "BSSWING (1160mV     (11) <Boundary Scan Output Swing, mVdfpp>, " &
   "         1030mV     (10)  , " &
   "         890mV      (01)  , " &
   "         740mV      (00) ), " &
   "CHPMFG  (Test       (100110) <Chip level manufacturing test > ) " ;


 attribute REGISTER_FIELDS of SerdesH : package is
 "init_data[6] ( "&
-- TDI
-- "*" = Value is required but deferred to BSDL level
 "(ALLBITS [6 IS  (5 DOWNTO 0 )  DEFAULT(CHPMFG(*)) NOPI  ), "&
 "(BSTERM  [3] IS  (5 DOWNTO 3 )  DEFAULT(BSTERM(*)) NOPI ), "&
 "(BSCM    [1] IS  (2)            DEFAULT(BSCM(*)) NOPI ), "&
 "(BSSWING [2] IS  (1 DOWNTO 0)   DEFAULT(BSSWING(*)) NOPI )  "&
 "      )";

end SerdesH;

package body SerdesH is
use STD_1149_1_2011.all;

end SerdesH;
```

New REGISTER_ASSEMBLY forms TDRs from IP Packages

```
use std_1149_1_2011.all;
use SerdesH.all;
use SerdesO.all;
.
.
attribute REGISTER_ASSEMBLY of chip_2011 : entity is
"INIT_DATA ( "&       -- TDI
"(USING SerdesO)," &
"(Array IO(0 TO 62) IS init_data DEFAULT.ALLBITS(CHPMFG(Test))),"&
"(USING SerdesH),"&
"(HIO IS init_data DEFAULT.ALLBITS (CHPMFG(Test)) ), "&
"(USING SerdesO)," &
"(Array IO(63) IS init_data DEFAULT.BSTERM  (BSTERM(CPflt)) " &
"DEFAULT.BSCM (BSCM(DC_CPL)) DEFAULT.BSSWING (BSSWING(1115mV))) "&
          ")";       -- TDO
```