Date – 12/20/2011

Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Carl Barnhart, Ken Parker, Craig Stephan, Dave Dubberke, Wim Driessen, Josh Ferry, Adam Cron, John Braden, Peter Elias, Carol Pyron, Bill Eklow, Heiko Ehrenberg , John Seibold, Francisco Russi, Ted Eaton, Lee Whetsel,

Missing with pre-excuse: Adam Ley,

Missing: Neil Jacobson, Mike Richetti, Ted Cleggett, Matthias Kamm , Roland Latvala, Roger Sowada, Dharma Konda, Sankaran Menon, Bill Bruce, Jeff Halnon, Brian Erickson, Kent NG

Agenda:

1. Patent Slides and Rules of Etiquette
2. Holiday schedule discussion
3. PDL discussion
4. Happy Holiday's!

Meeting Called to order at 10:30am EST **(new starting time)**
Minutes:
Review Patent Slide – Reminder sent out over email.

Solicited input from anybody who is aware of patents that might read on our standard.

No responses.

Review of Working Group Meeting Guidelines

No Objections

Holiday Discussion

Should there be a meeting on Dec 27,2011.

Carl moves to cancel meeting
Seconded
NO objections
Next meeting will be on 3rd of January
Friday meetings are canceled for the rest of 2011

Carl advocates to review the draft as much time will not be available when the draft goes to the IEEE for review

Believes the body is finished at this point. Annex B is mostly finished. The bulk of the work is going to be Annex C

Ken is concerned about the lack of time left for an in-depth review based on our current schedule

Carl: time to do it is dwindling if we want to meet out schedule to send to MEC, and isn't there for a full review of the draft

CJ: We are setting the schedule. Would like to be thorough. Our intent is to go through every thing. This process doesn't have to be in the meeting though. That is why we solicit feedback through email.

Carl welcomes the feedback and will make changes where applicable.

CJ welcomes anyone to bring up objection to any of the clauses so we can review the subject.

Carl: wants a review plan for the meeting on the 3rd.

PDL Discussion

CJ: has some concerns that there is an artificial rush created to settle PDL. And is creating some issues with PDL which has been in the standard for over a year.

CJ yields the floor to those that are opposed to adding PDL level1 (TCL) to the standard to discuss the problems and concerns

Adam C: Point is that .1 is about structure and never about what the communication consisted of to talk to the chips and board.

1687 is nowhere near done on pdl1 (personal opinion) and to think that we can start defining anything today that is better or more coherent than they have done over the several years isn't going to happen

CARL: so are you talking no PDL at all?

Adam C: the init group has defined PDL 0 enough that they can get the INIT section done. It's the adding of the looping and branching etc that is opposed

Wim: agrees with Adam. The level of PDL 0 is ok for INIT. That is the only place we need PDL for.

Ken: brings up INIT in a parallel setting. Has sent out a table to the group. PDL0 was suitable for INIT when it was simpler. If INIT is more difficult today than how would you parallelize chains doing INIT. Looking at the actions that need to be done would be a first step and not sure we have done this. It might be premature to go down the road as to what we need for PDL. Our init today is more intricate.

Bill E: Have we tried to model the init or some of the IOs that are current existing to see if it can be done in PDL0 solely so we don't need to go to PDL1.

Carl: what has been added to INIT recently is the power domain and with level 0 as defined in the standard you can do that because you need to read the segment cells to know if it is a 1 or 0 and then you have to act on the result. Can't make the decision in PDL0. Extensions are needed whether it is called PDL0 extensions or PDL1

Ted: sees many "we must have" statements for reasons to having looping. Not sure we must have anything. Don't have to have ECID that requires looping or Power Cells that have looping. Needs to support INIT. Don't need to run instruments in .1

John B: Feels the burden falls on the tool vendors. They are going to support the PDL1. He doesn't have an objection to PDL level 1

Wim: you have to look for what your goal is and look at what functions you want to execute. Need to know what to do in the sections you are testing. Need to do a number of steps to initialize your chip and wait for some parameters to settle. You only have to check if your Initialization was successful. Don't see any decision control there. No need for loops to do step by step procedure

Carol: We must support enough PDL to do INIT, power domains, ECID, and make it reasonable to parse and create. Any looping always gets flattened but makes it

easier. Need to work through some examples to see how much of a burden it is to having looping. Do like allow design flexibility and no restrictions on how to access the ECID. The access mechanism can be time consuming. Also dislikes having strong requirements for verification. Do believes that we need to get a standard out that will allow for some flexibility for the future.

Adam C: Needing PDL to turn power on or off is more than we already defined for INIT.

Carol: needs waits periods.

Ted: needs to weigh flexibility and usability

Carol: agrees. Needs to balance all of those things. Needs to work through some more examples to see where we end up

CJ: Our understanding of the challenges has evolved. Up to the working group if those challenges are something we need to address or not to address. Nothing wrong with learning as you go along and get a better understanding of the challenges.

Ted: Industry did realize these things and thought about .1 and decided to create a new standard that is to be an extension of .1

Josh: would like a standard way to do it (INIT) has to support multiple stake holders in the tests that he comes up with. To try and support lots of different tool vendors it is difficult. As an end user, desperately wants a standard way.

CJ: doesn't feel that we overlap 1687 to the extent that it is made out. Very little overlap. PDL1 in 1149.1 isn't the full PDL1 that is in 1687

Adam C: to see this comparison would be helpful.

Carl: As editor. We have added new capabilities to the body of the standard. Most of them require more than just BSDL and require some way to communicate to the user. Probably important to have a standard format to exchange that information. Should call it 1149.1 PDL not level0 or level1

Ted: Could redesign hardware that we have added to make them not require the complex language

Adam C: less is more

Ken : the dreaded flexibility

Carl: need to handle the software aspect of the hardware we are going to put in the standard.

CJ: Ted after the break will you show the working group how 1687 will address a PRBS board test?

Ted: certainly

Ken shows slides that he had sent out as email late last week

How do you parallelize this into a concurrent set of operations.

Table1 The Interconnect Test Process

Table2 Interconnect test with an Initialize preamble for 3 of 4 devices

Simple model before – INITSETUP, shift data, EXTEST, INITRUN, readout status(polling)

How does this process change when trying to parallelize all of these steps.

CJ: Original view point is that IOs need to be set exactly at the same time through update. Is that possible? Even for the functional part of the system? Is this a real solid objective that we need to obtain?

Ken: There are times when bad things happen so sometimes you need to be worried about when things happen.

Ted: degradation of IO cells can happen leading to early failures in the field. If you don't have a controlled environment in the test process you can get problems down the line.

CJ: board in front of him can't configure all the IOs at the same time.

Ken: true. But you need to be able to come up with a boot up process that is clear and consistent

CJ: we are creating this constraint

Adam C: when the board is coming up it is under functional control. Can monitor if the voltage is too high. In boundary scan you don't have control of these things.

Carol: There are ways to not have contention issues in 1149.1

Ted: large difference with system running at system speed and JTAG and running 100khz. When it needs many clocks this could be a huge amount of time.

Ken: We need to take a concept shown in table 2 and expand it to show the ramifications and it will lead us to show us if we need flexibility somewhere else. And this will need to be done before we go to far.

Happy Holidays.

Meeting adjourned: 12:06 EST.

Motion Summary
0 Motion Made

Next Meeting: 12/27/2011 11:00 AM EST

HomeWork Status

John has passed his examples in to the working group. CJ is running them through the parser.

Carol – is still working on examples
Heiko is still working on examples.
CJ is still working on port assignments

Homework assignments.

Heiko and Carol's assignments are outstanding and will be done for next week's meeting

CJ will have examples of port assignments
Bill E – work on more concrete example and definition of the ESSID register

NOTES:

1149.1 working group website - http://grouper.ieee.org/groups/1149/1/

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pppppp11491p*pp03820#

JOIN the meeting as GUEST – will have to ask to present

Meeting time: Tuesdays 11:00 AM (EST) (Recurring)

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