Date – 05/22/2012

Attendees: CJ Clark, Brian Turmelle, Adam Cron, Heiko Ehrenberg, Carl Barnhart, Jeff Halnon, Wim Driessen, Ken Parker, Rich Cornejo, Roland Latvala, Dave Dubberke, Dharma Konda, Francisco Russi, Hugh Wallace, John Braden, Carol Pyron, Sankaran Menon, John Seibold, Peter Elias, Bill Bruce, Craig Stephan,

Missing with pre-excuse: Adam Ley, Bill Eklow, Bill Tuthill, Roger Sowada

Missing: Lee Whetsel, Matthias Kamm, Mike Richetti, Neil Jacobson, Ted Cleggett, Brian Erickson, Josh Ferry, Kent NG, Ted Eaton,

Agenda:

1) Patent Slides and Rules of Etiquette
2) Use LiveMeeting "Raised Hand" to be recognized and take the floor
3) SysClk_Requirements attribute review from Friday
    a. Motion to accept SYSCLK_REQUIREMENTS attribute subject to editor modifications and enhancements
4) Finalizing for Ballot – What's left? (other than next two agenda items)
5) REGISTER_ASSOCIATION
6) REGISTER_CONSTRAINTS

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- No unary operators allowed in an M_I

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    a. CJ to get with Carl, Bill, Hugh and anyone else for wrap-up

Meeting Called to order at 10:30 am EST

Minutes:

1) Review Patent Slide – Slide Presented to the Group.

Solicited input from anybody who is aware of patents that might read on our standard.

No responses

2) Review of Working Group Meeting Guidelines

No Objections

3) SysClk

CJ – Attributes “nailed” at Friday’s meeting; Carl crafted edits; CJ showed edits

CJ – Can list Instruction that goes with SysClk requirements

Carl – Port ID, min freq, max freq, IR, multiple clocks; otherwise, no new data on this other than what is in the draft, now (PDF sent out)

Ken – Line 8316?

Carl – “… as always, can use clocks as you want…” was probably what Carl wanted to say.

CJ – a), b) (line 8332) is probably not the right restriction. Need to have the package file mod at the “sub” level. Otherwise, top-level BSDL would mess this up

Carl – how to tie off a system clock

CJ – Recall that user-defined IR might need a SysClk, too.

Carol – Different packages (chip bond out) needs flexibility. Test mode may have different needs than mission mode.

CJ – Carol’s second comment is about b). Clocks are not tied to the CHIP, they are tied to Instructions. Example: ECID is ON in one package and off in another.

Ken – If open on pin for clock needed for INIT_SETUP, then that won’t work. Ken thinks that if something is shipped as not working, then a BSDL should reflect that and remove the non-working items.

CJ – But you can’t edit the BSDL in that area. Can only mod packages or add packages.

Carol – Ports may not be used in all packages.

Carl – PDL won’t work, and how does user GUESS that certain things don’t work in the context of missing ports (for example). Need a context switch. Ted’s idea may be it…

CJ – iGetPackage

Carol – INIT_SETUP has 3 clocks… Main, pex1, pex2. 1 package has main, pex1. 1 has all clocks. Need some way for INIT_SETUP to swap between PDLs, etc. Need 2 ID codes?

CJ – Multiple pinmaps. But this does not work well for tie-offs. Now we are back in this granularity issue with INIT_SETUP: So, need IR granularity AND package granularity. Small package will be missing some pins, so PDLs need to be skipped/edited to make this work. Tools can't make this decision based on BSDL… Register value may be the "branch" mechanism… Unconnected clock inputs break things with the current rules.

Carol – Still sees an issue. Need a way to associate a clock to a register segment.

CJ – R_A could be a solution.

Carl – Does not help solve a "generic" PDL situation.

CJ – Package determined by board-level netlist or by inputs from tool (user) that tell tool what package is to be used. So, tool should know the package type.

Carl – So, no way to look ONLY at a BSDL and guess the package.

CJ – iGetPinmap would be better.

Carl – Could just pass package in at runtime…

Carol – Need to do an IF statement, so Level 0?

Carl – No, this cannot be Level 0.

CJ – If parameter came in, then no branching, but could unroll based on some register field.

Hugh – Singing 1149.1 praises to P1687 WG. BUT, getting bogged down, now. Is there a way to summarize the features and work from bottom up?

CJ – Sounds like a new agenda item…

Hugh – Heard "IF statement"; do you want to standardize that "IF"?

CJ – New topic…

CJ – Could pass in a parameter. But, need level 1.

Hugh – Or a level 0.5…

CJ – So, removing b) (line 8334)?

Ken – Uncovered an issue, but deleting b) does not SOLVE the "can of worms".

CJ – b is too restrictive.

Carl – Or, we leave it in and figure out how to solve this issue.

CJ – CAN use single BSDL, but b) restricts this. Branching CAN be done…

Francisco – Agree that this should not be in the pinmap string, but could be in port declaration?

CJ – Maybe "at least 1 clock cannot be OPEN, TIEx…"

CJ – Back to a) (line 8332):

Carl – Would like to see a port declared as a CLOCK…

Ken – Early days needed INTEST but had observe-only on clocks.

Carol – COULD make a bidir a clock…

Carl – Could add OUT.

CJ – To make this work, need to go into BSDL file and call some pin a clock so that this attribute can work… Can SNPS spec a Function "CLOCK" for example?

Carl – Focus is on verification. Without some spec, may have a test issue, but won't be found. If BSDL is like documentation, then should be able to document system clock in BSDL.

Carol – Withdraws comment.

Dave – May never have OO cells at all. May be declared as linkage.

Carl – Sounds like NON-compliance…

CJ – Diff-clocks are analog…

Carl – It is a documentation question. Sure, there is a future direction in chip design, but need to be careful about this and not allow "skimping" on docs just to pass validations.

Francisco – Port not a clock, it is IN, OUT, etc. Function not defined for CLOCK.

CJ – Need consistency. This says clock must have a BS cell. A) adds new requirement to add a BS cell on that input.

Roland – Also uses diff clocks and could float one side and run single-ended. Need rule to support diff nature.

Carl – Rule c)…

CJ – Not trying to make a standard that is ill-defined. THIS rule seems to go a little FARTHER…

Ken – Proposes bifurcation of rule.

Carl – Is it OK to list clock as linkage? Is that compliant, today?

Ken – People lie all the time…

CJ – Analog pin is the "out" or exception. Could be one of the new LINKAGE_* port types.

Carl, Carol, Ken, CJ, Hugh – Seem to settle out on solution… For a), anyway.

Francisco – Add a pin type called Clock…

Carl – Clock IN, OUT, … Would rather use function and save port as PAD type, not function related. Still need to hash out b) issues related pin map and PDL issues, etc.

Ken – … So, IC vendor would provide tool to test generator for these situations?

CJ – Yes.

Ken – So, 100 chips, 50 tools… Thought tool vendors (not chip vendors) would provide these tools.

CJ – IC vendors are proving tools like this today. Like FreeScale IMX (53) chip has a configuration package.

Ken – Doesn't this new INIT feature set solve this problem?

CJ – We do not preclude that from happening, but also would see other tools, still.

Hugh – So, just need the output of some set of tools which would BE the INIT* info (PDL).

5) R_A

CJ – Proposal to make R_P_A just a more generic R_A to accomplish some goals like the clock/package issue we were talking about earlier. So, Register to PORT, INFO, USER type tags.

Ken – Single-word, multi-word list needs some definition.

CJ – Might be X-Y lists, System clocks, just a string.

Ken – So, info that A HUMAN might find useful.

CJ – For User, yes. Though COULD be parseable.

Carl – Could be used for diags. Tool does not have to really understand the content of the tag, but could just dump it out.

Hugh – Is this related to alias or attribute in P1687? Like a number?

CJ – Number (in this case of the example) is a coordinate in the die.

Francisco – Path would be more useable compared to physical location.

CJ, Carl – This can be anything.

Adam – Seems loose… Extensions and BSDL is rigorous wrt/actual hardware, etc. This is wide open.

CJ – actually, this puts more rigor than syntax of BSDL extension. It's optional and intentionally wide open.

Carl – sees this as a way to move random stuff (docs) to a more useable format.

Meeting adjourned: 12:00 pm EST.

Summary of Motions Voted on
0 Motion voted on

Next Meeting: 5/29/2012 10:30 AM EST

NOTES:

1149.1 working group website - http://grouper.ieee.org/groups/1149/1/

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Meeting time: Tuesdays 10:30 AM (EST) (Recurring)

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