

August 03, 2010

Minutes of IEEE 1149.1 - Initialize Sub-Group Meeting

Attendees:

CJ Clark  
Dave Dubberke  
Roland Latvala  
Ken Parker  
Carol Pyron  
Carl Barnhart  
John Braden  
Francisco Russi (taking minutes today)  
Brian Turnelle  
Craig Stephen  
Win Driessen  
Neal Jacobson  
Heiko Ehrneberg

Minutes: CJ open the section at 11:02 AM CST

In this meeting Neil Jacobson was introduced by CJ as a new member with long industry expertise in 1149.1/.6, follow by a brief personal introduction.

Welcome to the team Neil.

- CJ review last week's topic of discussion about the hierarchical BSDL and register mnemonics and segments from Carl, and mentioned the need to work on the dot1 BNF. Also reference the analysis done by Bill Bruce on ICLs
- Carol INIT BSDL mostly stable need to drive into the BNF,
- Carl need to make changes to registers fields, addresses and field segments
- KP to review a new issue about disabling differential drivers' and the state of the positive leg and the negative leg when the driver is disabled, possible missing information in the dot1. This was raised by a discussion among KP and Stephen Sunter.
  - The meeting evolved around this topic
  - KP presented the email exchange with Stephen as the introduction to this problem:
  - When a driver is disable should the state of the positive leg and negative leg be Z, weak1 or weak0, LVDS typically goes to Z, if drive up done with a 50ohms resistor, and drive down with a transistor, then it may be strong1, if using a single enable to disable the driver, then should both legs pos/neg be Z or Pull1 or Pull0? When the differential driver is disable then both legs go to Z, but nothing is implied about the negative leg, BSDL describes the positive leg, in the dot6 STD the negative leg is the same as the positive leg when the driver is disable, but it is never discussed in the dot1, must describe this behavior for the benefit of those making the tools, for single ended drivers it was understood that one driver was disable but another may be driving, multiple drives acting, i.e: wire-and, wire-or as oppose to tri-state, today we have several voltages and buses pins, no interpretations in BSDL if differential driver is Z and have a valid hi/low on the two leg to verify, or it is unknown downstream.

- John receiver –driver side disable
- KP pulling behavior was relative to the negative leg, two assumptions KP vs. CJs
- CJ ask KP if he has a proposal.
- KP in silicon both legs go to high or low, a Pull0 that mean both legs go to 0; is there a case where they go to complementary values?
- CJ preferred everything to resolved to Pull0 or Pull1, if output Z it is difficult to resolved, LVDS difficult circuit to get a fail state: i.e: PCIe, to detect an open then you need a pull behavior
- Carol the receiver default to a value, not the same is 3-state, there is variability to this issue, all drivers are 3-state, then you capture an X, predicts only on X
- CJ minimum value not usable if all you have is Z
- Carl Pull1/Pull0 on positive, what about negative leg? If all drivers are disable, then hard to predict
- CJ (ask if Dave was in the meeting) present the old figure where both legs are biased with EXTEST, a BC\_7 for data\_in and a Control cell on the differential drive bidir enable,
- KP there is no way to describe the negative leg in the BSDL, both will be Pull-up, but it is not stated in the dot1, it is a new concept to use biased resistors for both legs, a small leakage then the PU/PD will take over.
- CJ ...
- Carol LVDS receiver only, or bidir as shown
- CJ any place, bidir as well, predictable response, high speed friendly, only when we are testing we get this capability, we don't need to describe the negative leg, electrically we need something there
- Roland should it be HIGHZ, and not EXTEST for biasing
- CJ yes, may be valid, can't generate if 3-state
- Roland why EXTEST?
- CJ deterministic
- Roland Highz or EXTES are deterministic, both legs same polarity unpredictable results
- CJ not relying on observing the receiver, need EXTEST, not design to do that on control cell, 0/1 all can receive.
- KP bidir have simple drivers, two FETs and two resistors
- CJ no, it is a feature of the receiver
- KP if we have a receiver structure, and no R, is there a descriptive way to tell that?
- CJ we need a way to describe this on a receiver
- KP do we tell people to use a resistors on both sides?
- CJ introduced the concept of in0 in1
- Roland if designer does not add PU/PD then is it inX
- Carl Yes, it is the default behavior
- CJ don't think we should be counting on PU1 PU0 to give us coverage
- KP devices with PU1 PU0 Z mixed on the same bus, some may have leakage, how do I predict state, we may write on incorrect test, then lost of debugging
- CJ not see this anymore, a simple construct today may be better to have in1 in0
- KP differential receivers assign differential levels that are open in1 in0, if open on one leg of differential the hat does it mean?

- John what do we predict
- Carl dot6 covers this
- KP dot6 dived the problem into two, yes dot6 is the way out, but need guidelines to write a test for out of the box quality
- Carl out the box, assigned an X to all receiver that are not driving
- KP if I am not in control, then do not match in reference
- Carl make assumptions, then it does not interact at all in0 in1, will not interact PU1 PU0, will interact at the board, anybody can put ? to capture faults on differential drivers
- KP single ended, no choice
- Carl why do you rely on Pull
- KP how do I reliable look at pin, differential can make fairly assumptions when both legs are the same, disable legs would have Z or same value, an assumption is no longer value
- Carl I like to make a proposal, if differential driver Z, no information present, if different value, code as PU1 or PU0, and some drivers may be acting down the stream
- KP some error to that proposal
- CJ need more clarification
- KP we need to ask for help to the design community, both pins disable hi, call that Z
- John what is expected?
- Carl Z no info transmitted, PU1/PU0 implies information, but no transmission is happening, new description for BSDL
- KP need to change the BSDL
- Carl must be compliance to 2011
- CJ, Roland, Carol and Dave to get advice from real silicon designers
- KP moving away from a single ended going into bidir on both ends, would not see 25 of them on a single wire, if separately some would be Z, is that real
- Carl CML terminates on 50 ohms resistor, all driver can override this resistors
- CJ then mission mode is off for the bidir, need good examples
- KP, Carol, Carl will take on BNF next INIT meeting, others don't have to attend, CJ ask to be included
- CJ one AI to ask for help to differential drivers designers about this issue
- CJ call to adjourn the meeting at 11:04 AM CST, KP second the motion

Note1: KP has send two follow up emails after the meeting ended in regard to the new issue; I am attaching bellow these emails for your reference in regard to the minutes:

#####email from KP-1#####

Hello Dot1,

What I heard today (from Carl) was that we should offer guidance in the standard about how to encode differential drivers in BSDL with respect to Z, Pull1 and Pull0:

1. If the differential driver enters a high impedance state on both pins when disabled, then code it as 'Z' indicating no information is present.

2. If it produces a 1-0 pattern on the two pins, code it as Pull1; a 0-1 pattern would be coded as Pull0. There is an assumption here that on-board pullups, or downstream pulling function in other devices, or combined leakages would not materially change these states. (I'm a bit nervous about such an assumption.) The implication of Pull0/1 is that there is static but valid information on the driver legs when the driver is disabled.
3. If a disabled driver has BOTH legs go high or both go low, then any downstream differential receiver cannot sense meaningful data (no information is present) and thus the driver should be coded as producing 'Z', even though it is not truly in high impedance. Thus, we are saying "there is no information present on the differential pair".
4. If you have a device that follows option 2) above, but you are nervous about the stability of the Pull0/1, then code such as 'Z' as well.

So, we have an existing body of devices and BSDL out there today. What have we got on our hands right now?? How many BSDLs in existence today would (per the above) have to be changed?

Regards,

-ken parker-

#####email from KP-2#####

Hello Dot-1,

I perceive a weakness in 1149.1 with respect to differential pin pair behavior when differential drivers are "disabled".

Right now, in BSDL we describe the positive leg and its relation to the BReg, and there is a description of what the disable behavior is for the positive leg when such behavior is implemented. In a nutshell, we say the positive leg goes to 'Z', or a weakly pulled 0/1 state.

But, what does that imply about the negative leg? I have only recently confronted this question -- my assumption was always, the negative leg matches the behavior of the positive leg when disabled. Thus, if the positive leg pulls weakly to 1, then so does the negative leg. If the positive leg tri-states, then so does the negative leg. Finis.

You can see from a discussion I had below (with Steve Sunter) that this assumption seems to be largely true for designs such as LVDS and CML. But, I worry we have not really thought this through and sought enough expert advice. We do not teach about this in the standard, nor does BSDL really explain what it is describing either.

In my opinion based on the history of Dot1 since 1990, a disabled driver of any kind does not transmit information, whether it goes to Z or a 0/1 pulled state. What the disable means is that another driver sharing the same communication path

with the disabled driver, can assert its own state successfully. If we have only one driver and one receiver on a path, then when the driver is disabled, we may not be able to (in all cases) predict what the receiver sees. In the differential case, two Zs, two 0s or two 1s cannot be reliably interpreted at the differential receiver. Thus, there is no data transport. But if there was a driver out there that pulled one leg high and the other low when disabled, and you know this, then you could argue you can predict receiver performance. But, I'm not sure this is reality, and we should not predicate testing on such assumptions.

Should we discuss this issue, and can we improve the standard with a better treatment of this issue? Right now, we've got some glaring holes.

Regards,

-ken parker-

-----Original Message-----

From: Sunter, Stephen [mailto:Stephen\_Sunter@mentor.com]  
Sent: Sunday, August 01, 2010 11:02 AM  
To: PARKER, KENNETH P (A-Loveland,ex1)  
Cc: carl.barnhart@SILICONAID.COM; beklow@cisco.com  
Subject: RE: Disabled Differential Drivers

Ken,

In most cases, when both legs are tri-stated simultaneously (only one enable signal). However, we saw the ability to separately tristate (to Z) each output in Intel's driver (April 2009 meeting).

In the case of a typical LVDS driver (transistors perform both drive up and drive down), tri-stating it would deliver Z on both outputs.

For a CML driver, if the drive up is accomplished with a 50 ohm resistor, and drive down is accomplished with a transistor, so tri-stating would deliver a full-strength pull-up on both outputs. (There could be a 100 ohm resistor across the pins at the receiver end, so the nets would only be Z from a BSDL point of view.)

Sometimes the CML pull-up resistor is implemented with transistors (to permit tuning to 50 ohms), in which case it would be possible to deliver Z on both outputs. Other times the 50 ohms is implemented with multiple resistors in parallel to permit this tuning, but this still prevents Z.

In summary, with a single enable signal, both outputs would go Z or both would go pull1 (or pull0). In a driver like Intel's, each could go to Z separately. So, anything goes.

BTW, I'll be on vacation Tues~Thursday this week, and radio silent.

.../steve

-----Original Message-----

From: kenneth\_parker@agilent.com [mailto:kenneth\_parker@agilent.com]  
Sent: Friday, July 30, 2010 5:34 PM  
To: Sunter, Stephen  
Cc: carl.barnhart@SILICONAID.COM; beklow@cisco.com; kenneth\_parker@agilent.com  
Subject: Disabled Differential Drivers

Hello Steve,

Here's a question about Diff Drivers.

Say you have one, and it can be disabled. In the BSDL BReg description we only describe the positive leg. Its disabled states can be Z, Weak0, Weak1, Pull0 and Pull1. My question is, what would the negative leg be doing in these cases?

My academic's view would be for Z, both are Z. For Weak0/Pull0, both go low, and for Weak1/Pull1, both go high. But is this true in practice??

-kp-

Note2: if any of this information needs to be expanded or edited, please send your comments directly to me and I will revise the minutes.

Best Regards,  
Francisco J. Russi.

=====