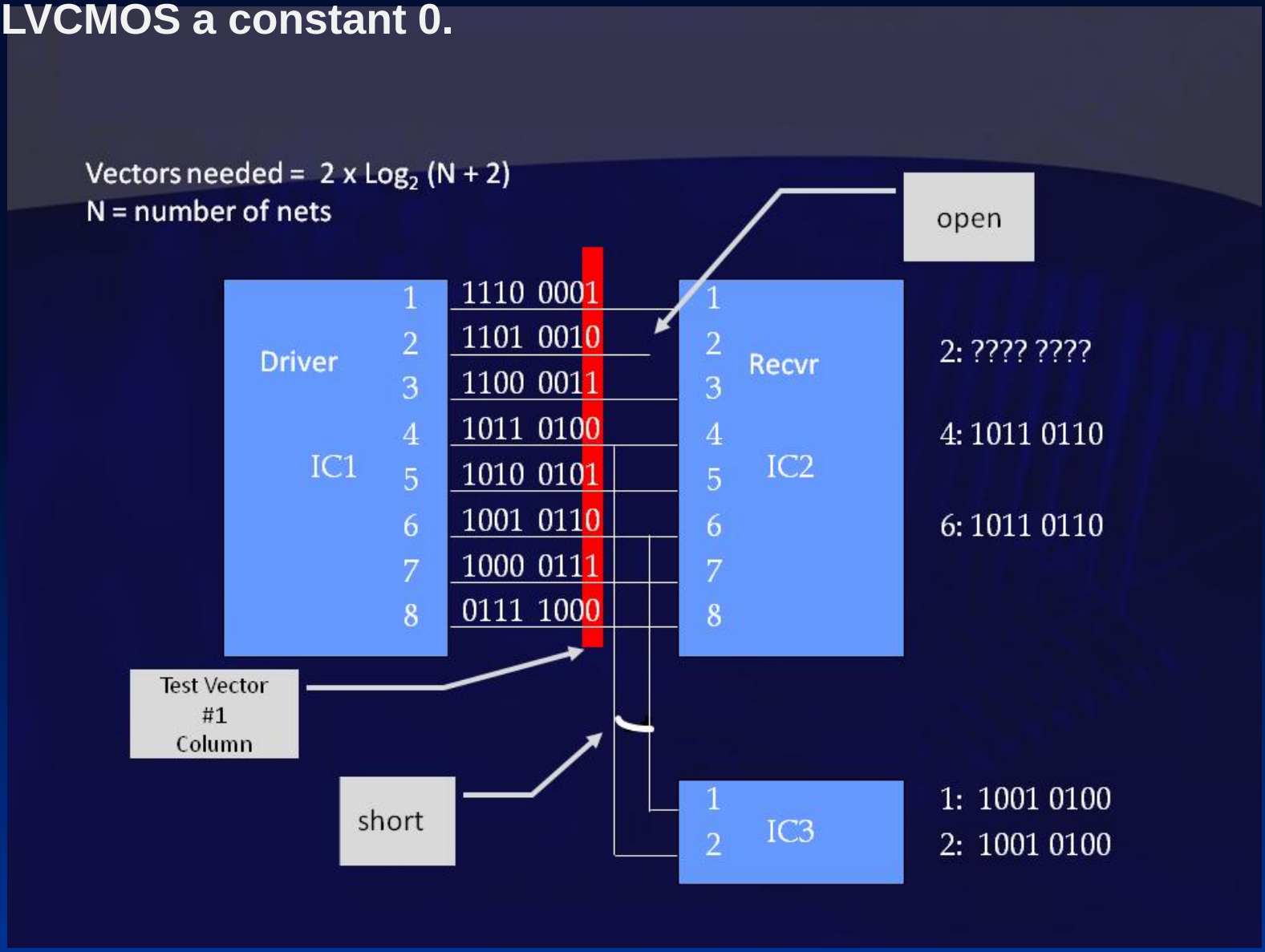
Understanding the <input spec> proposal For IEEE 1149.1

CJ Clark

Intellitech

Historically, OPENS have been diagnosable with 1149.1
As the value received at node 2 is constant, 99.9% of the time
And over temperature. LVTTL tends to give constant 1 and LVCMOS a constant 0.



Historically, the PULL value of an INPUT has been known On BIDIRECTIONALs.

" 397 (BC_2, IO_N3, output3, X, 396, 1, PULL1)," & -- PAD339
" 398 (BC_2, IO_N3, input, X)," & -- PAD339

While there is no specification on Cell 398, the specification on Cell 397 enables ATPG tools to predict the value present when The net is undriven.

- **Single point net**
- **Connector and pin IO_N3**
- **connection to other bidir pin with PULL1**

While "Z" is allowed in the standard, it has no usefulness in ATPG. It should not be used on future BSDLs. Since BIDIRs Can be 'undriven inputs', typical IC design would not allow a BIDIR to be un-biased at ALL when the BIDIR is in INPUT mode. (That would require lots of external resistors).

PCB trace affects the OPEN1/OPEN0

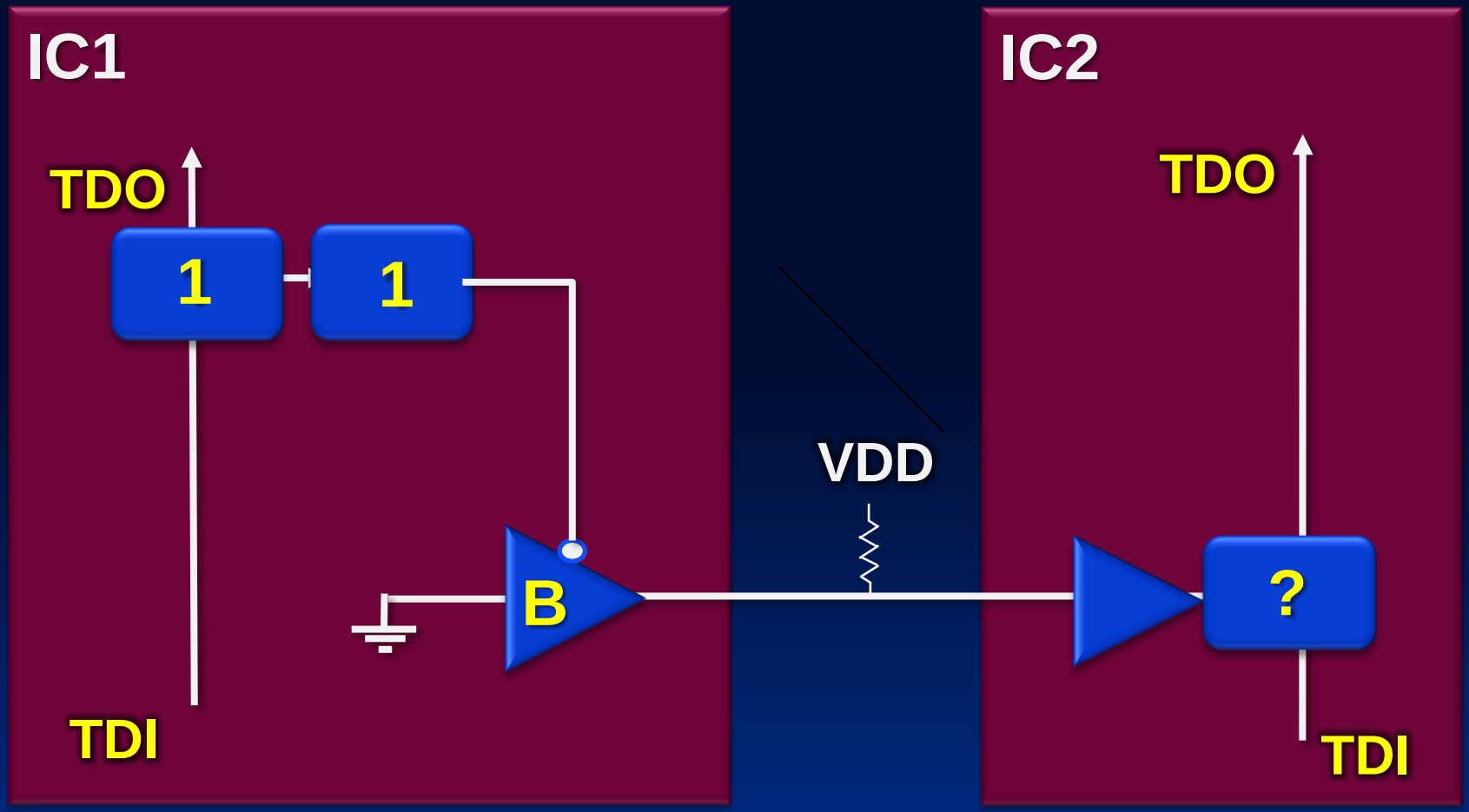
PCB top/bottom layer trace is about
2pf/inch.
Internal layers about 4pf/inch using common
Factors such as 6 mil 1oz copper and 12mil
Separation, FR4 and a E of 4.3.

Those can change, but not by an order of magnitude.

The intent is the OPEN1/OPEN0 for an open pin, it is understood
That ICs with perhaps 25pf of trace connected to them, may
Not achieve the OPEN1/OPEN0.

2001: OUTPUT2 with WEAK1 Description

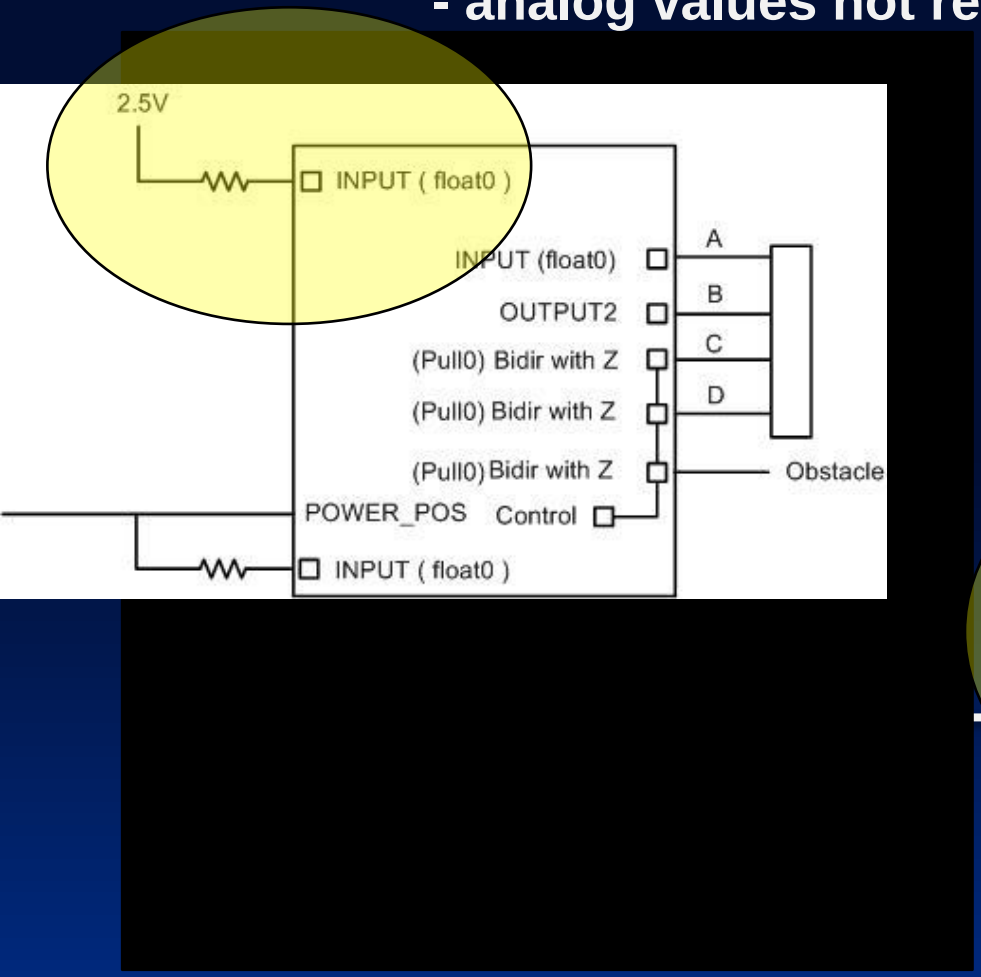
BSDL: "6 (BC_1, B, output2, 1, 6, 1, WEAK1)," &

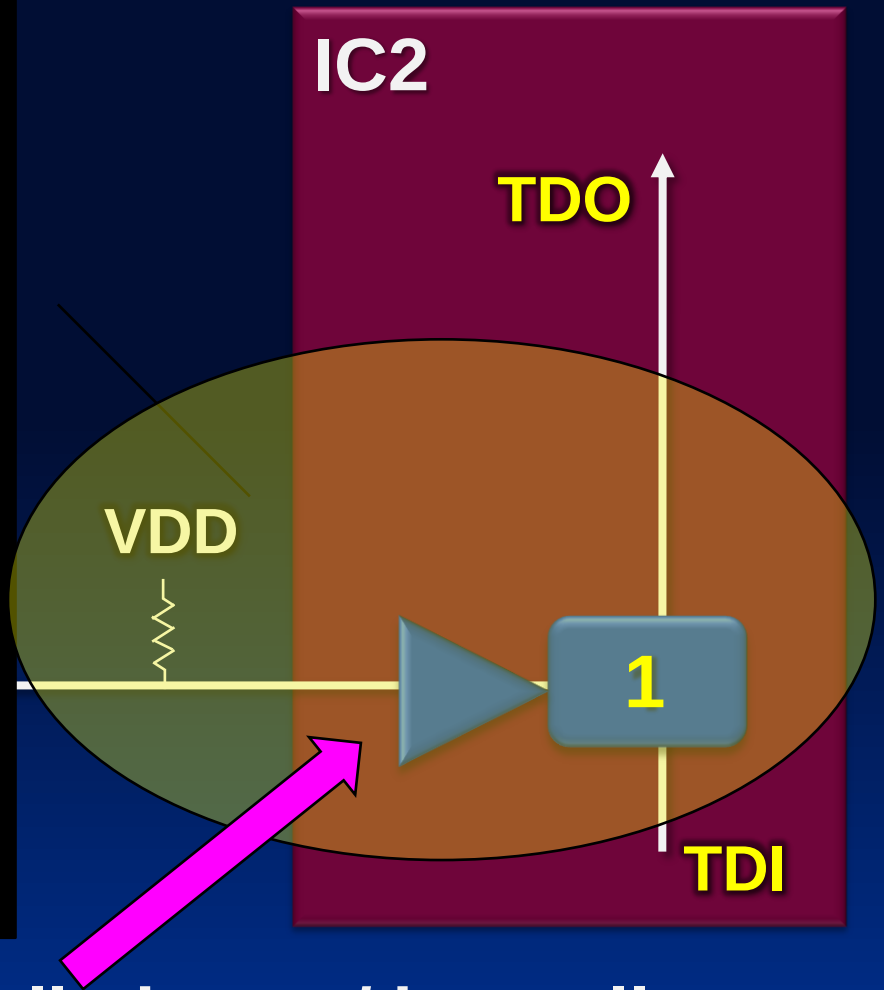


ATPG predicts a Logic 1 – well known
Voltage at VDD or resistance precise resistance value not needed

Comparison of draft figure and WEAK1

- with driver (covered) OFF the WEAK1 looks very much like the pull-up in the draft
  - analog values not required for 99.9% constructs

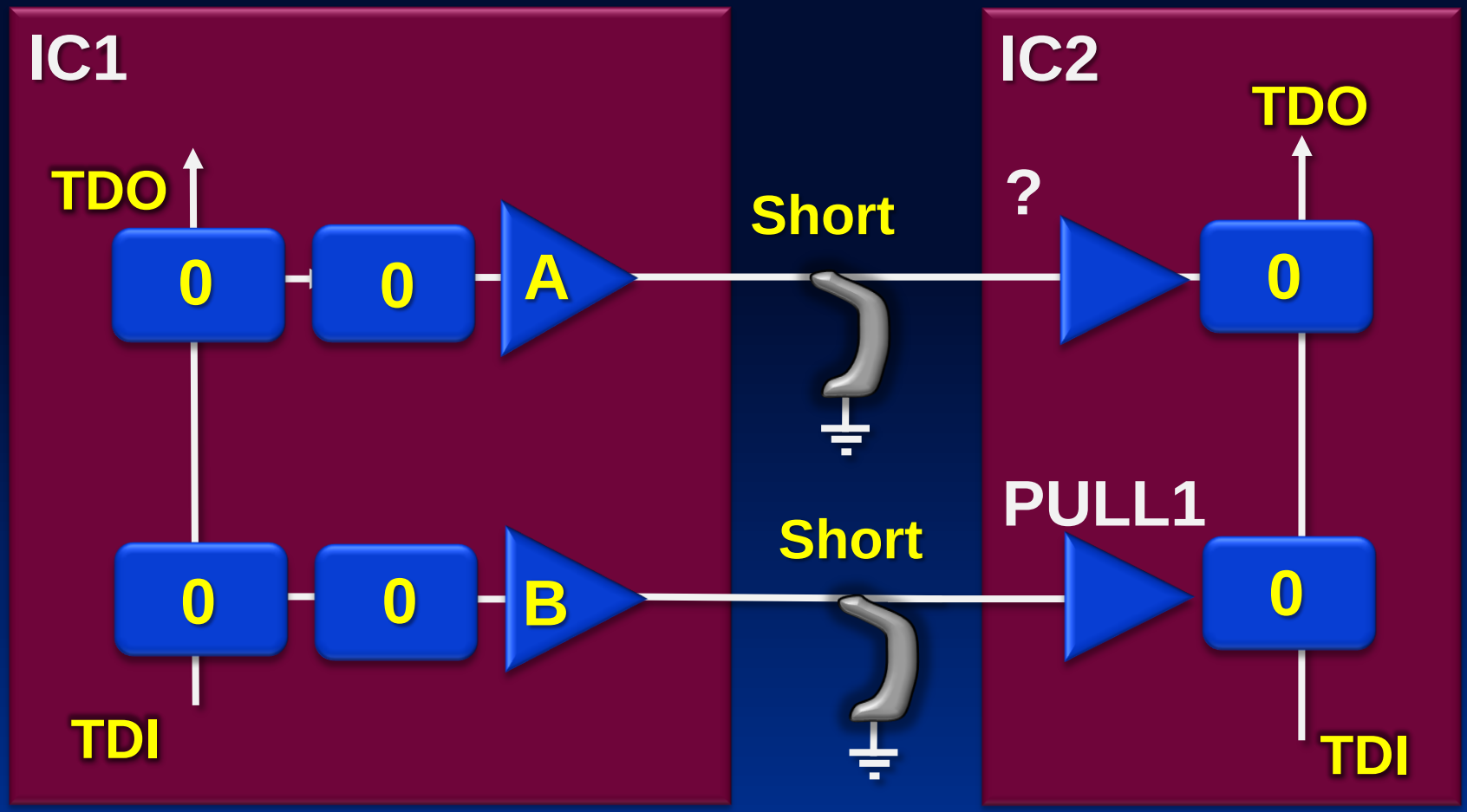




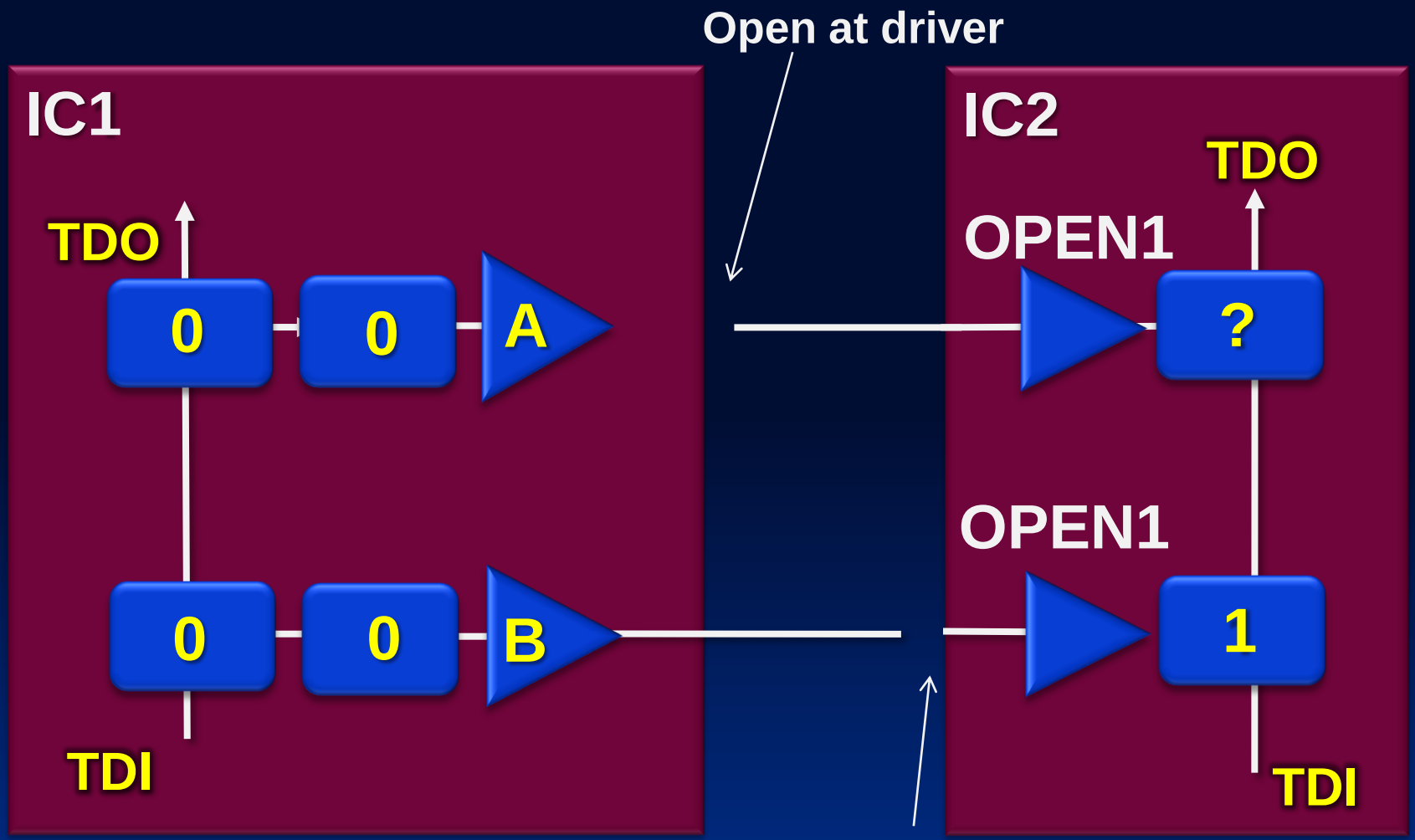
Input pulled-up w/ b-s cell

Better Diagnostics

2001 – input is unknown: “Net is stuck at 0 or open”
2011 – input is PULL1: “Net is stuck at 0”.

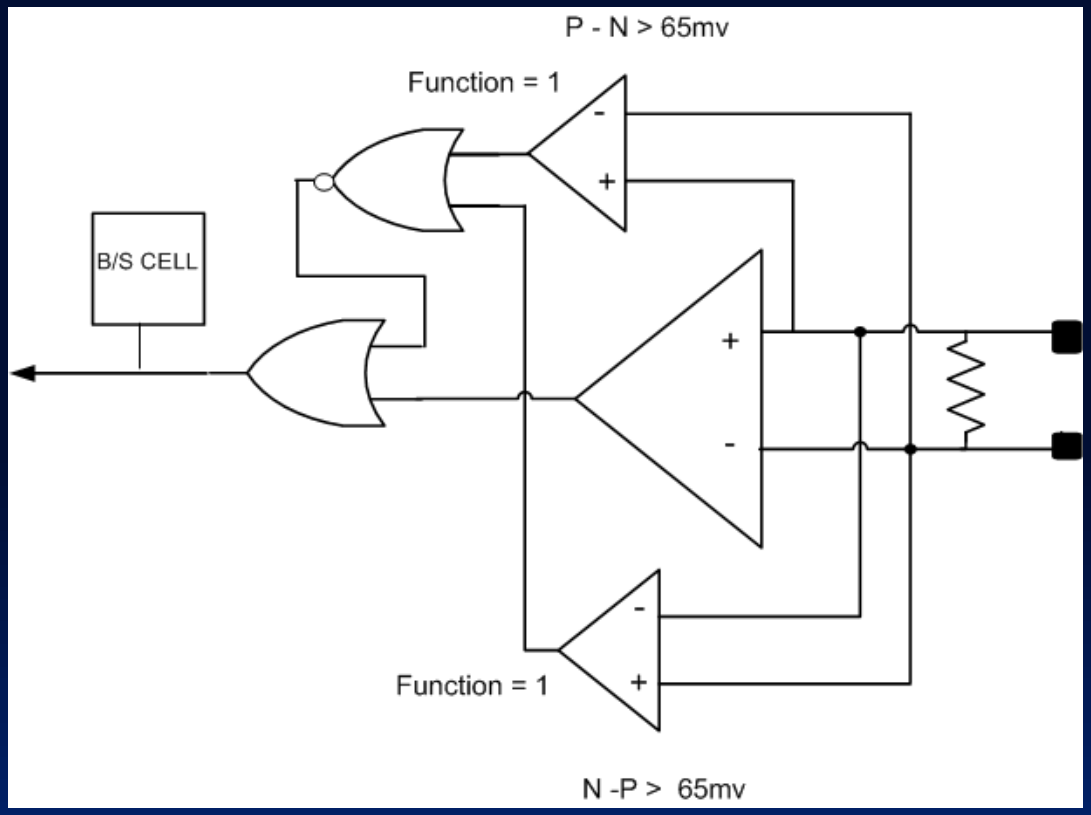


A non-constant value, perhaps induced by noise/cap on the long trace means its not an open at IC2 - that's useful for repair



Open at receiver

PULL1 does not have to be passive

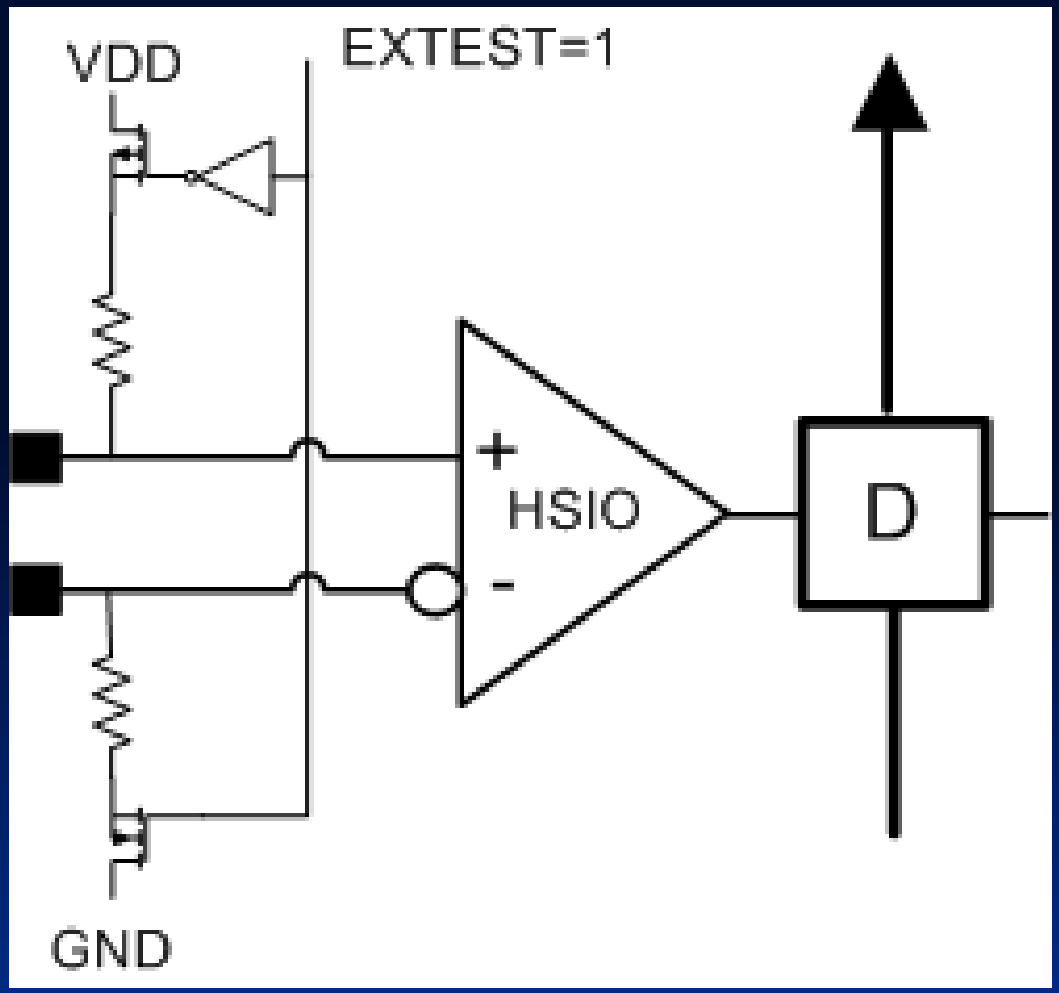


LVDS requires open inputs to cause differential receiver to drive ‘1’

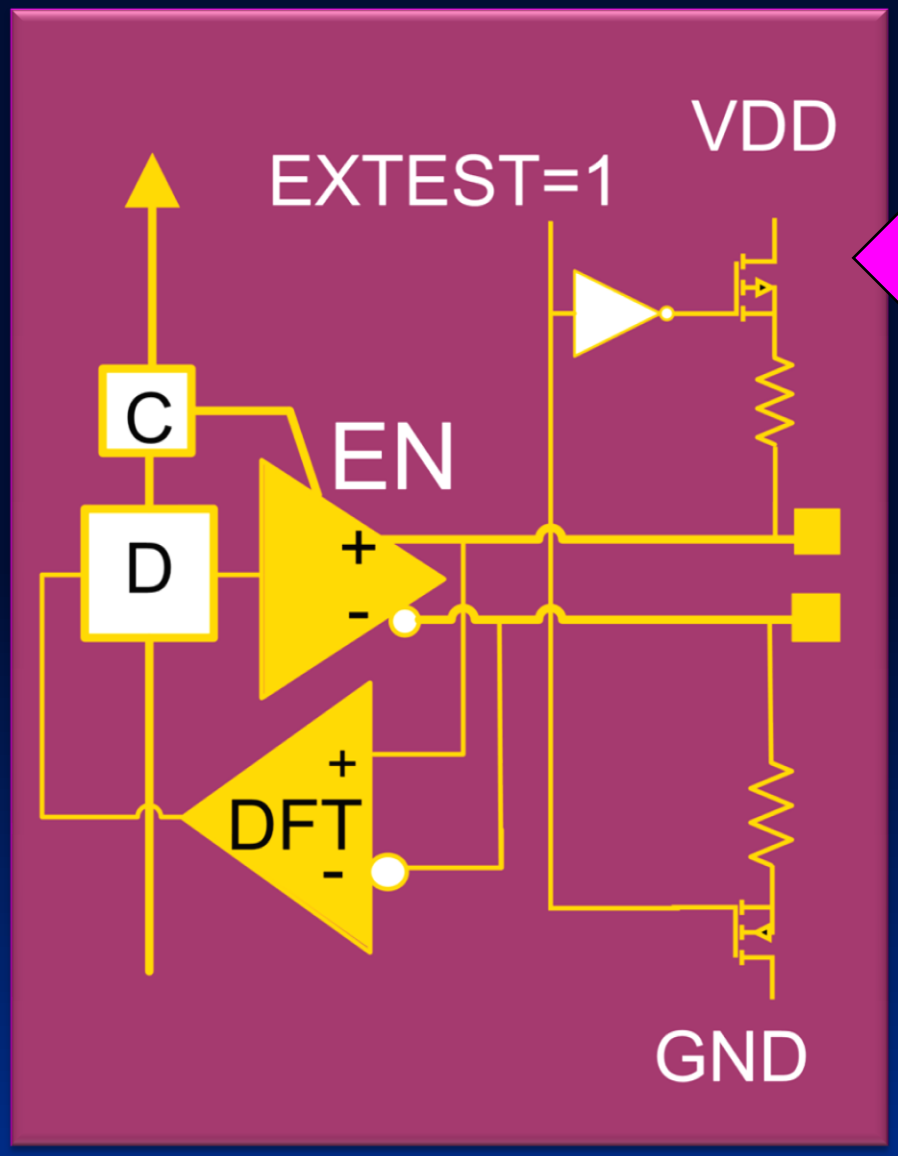
PULL1 satisfied by functional constructs

Bias only needs to be present during EXTEST

- HSIO output a ‘1’ when input pins unconnected and in EXTEST



HSIO with ‘pull1’ for EXTEST only
- PULL1 can be active such as done with LVDS



p-channel MOSFET

Slight receiver bias during EXTEST enables “1” capture for un-driven nets

n-channel MOSFET

“My inputs float”

New construct OPEN1/OPEN0 (formerly FLOAT1/FLOAT0) describes behaviour of Un-connected pin, an open pin.

- **Despite schooling on Complementary MOS, in real designs the input is affected by ESD protection, etc. The input goes one way or the other in 99% of the cases.**

Input pins in in a IC design, where inputs are part of features optionally used by the IC customer always be biased by designer.

- **keep away from Vref, remove external resistors for customer prevent unwanted support calls when customer forgets, prevent noise, and prevent excessive power consumption**

IC Designers should consider that inputs, normally driven when the IC is used, may benefit from a programmable pull-up/down for test modes. During PCB test, connectors exist and many inputs may not be driven. on-chip and at-speed JTAG tests may fail from noise.

There are exceptions, there may be inputs which are truly random, However these are few, 1149.1 OPENS tests have never been Diagnosable with such an open.

Designers can choose from a number of I/O libraries

LVCMOS inputs

- **‘plain vanilla’,**
- **with PULLUP or PULLDOWN**
- **programmable pull-up/pull-down**

- the latter is useful in obtaining low power, better signal integrity but maintaining test objectives

Understand that ‘no bias’, where an input hovers and switches around the input threshold (1/2 the scale of the input voltage) consumes more current.

During production PCB test, inputs to be driven in mission mode may not be driven
- socketed IC, missing mezzanine, connectors etc.

Advantages

DFT:
Analysis can be made when external pull-up resistors are not needed
Analysis can be made when external pull-ups pull to opposite direction

Fault Coverage:
Pull up/down on single INPUT, can determine if fault coverage exists
‘coverage exists when open input is at opposite state of pull’
Undriven opens (connector, non-b-s device) can be tested for shorts to other driving nets
Undriven opens can be checked for stuck-ats to opposite OPEN/PULL

Diagnostics:
Nets with single observe points (driver-receiver) can determine STUCK-AT rather than OPEN when opposite sense of input is fault
Nets with single observe points (driver-receiver) and OPEN1/OPEN0 can determine driver or reciever open when INPUT that should be A constant 0 or 1 is NON-constant.

But what about…

Many ‘modes’ of operation exist for PCB ATPG today.

User can simply select to skip the common 2001 PULL-UP/PULL-DOWN test done for bidir/Asymmetrical nets

For 2011, use the BSDL construct the way you best see fit
- without <input spec> everyone has NO choice but pin-by-pin manual entry

ATPG can be run in conservative mode via software switches

For instance:
- don’t include OPEN1/OPEN0 INPUTs for consideration during ATPG
- ignore OPEN1/OPEN0 INPUTs connected to disabled non-1149.1 parts
- ignore OPEN1/OPEN0 INPUTs connected to passive connectors