

1149.1 Working Group Meeting Minutes. December 8, 2009

Attendees:

Adam Ley
Bill Tuthill
CJ Clark
Heiko Ehrenberg
Ken Parker
Dave Dubberke
Adam Cron
Francisco Russi

Agenda:

Multiple Device IDs per BSDL
Linkage in/out
No Connect support for multiple bond outs of single die
Call for New Business

Minutes:

Meeting Called to order at 11:04am EST

1. OLD Business

a. Device ID

Ken had brought up Device ID

CJ – one and only one Device ID per die

Adam L – right or wrong manufacture will choose id on bonding out to package.

Ken – Second source of same die. Second manufacturer has a different id. This is seen as second source.

CJ – should be a separate bsdL per device. Multiple device id's per part is not in spirit of Device ID

Adam – multiple sources of same device and id reflects different sources of same die

Ken – different versions will have different ID but same bsdL. Why have unique bsdL per rev when one bsdL can cover it.

CJ – origin of bsdL is with manufacturer of device

Device ID described in standard as a ID for a single device.

Trying to do a board level functionality by supporting multiple

Device ID codes.

Ken – multiple ID codes are an advantage. One test that can operate with multiple chips.

CJ – Question is should decision and multiple device id's be part of standard and bsdL

Multiple Device ID's are more of a test engineering problem of describing multiple chips on a board level.

Ken – tools have dealt with this for many years.

CJ – disadvantage – multiple device ID. One can not predict what the device ID is from a specific BSDL. BSDL represents multiple devices and can not predict which test patterns to use.

Section 1.3 on purpose of BSDL

Ken – Read 32 bits and ignore the locations that are different between ID's. Would be represented by X's. This represents a change in sequence numbers. 30 bits of deterministic patterns and 2 bits are ignored. Possible illegal pattern that could be generated. This is a small possibility .

CJ – if only 2 bits were different that might be ok.. But typically manufacturing bits are different and those are more than 2 bits.

Ken – Feels number of different bits are acceptable compared to having multiple BSDLs.

CJ – can be managed outside the bsd. Don't want to promote hand editing of the bsd by test engineers.

Adam L – doesn't think it is a problem that has just come up. Has existed for a long time. No obligation to use facility at any level.

Ken – single bsd for two different packaging options. Helps with file management when you can have single file

CJ – all we are trying to do is review items and see what needs to be adjusted if any. Some items don't line up with other items and may need to be reviewed and that is all we are doing here.

CJ – Problems can be solved with tools. If we feel that one BSDL with multiple Device ID's are better than we can leave it as is.

CJ will write up an email to describe the problems better

b. Linkages input parameters. Is it an Output/Input

Ken – still wouldn't know what to do with a linkage input because ATPG doesn't know what to do. If it is a linkage output, there could be a conflict. Now you have a choice to test that net, Could put out warning that the pin wasn't tested. Or if you test the net it could cause some interference. Knowing it is an output raises a flag but still don't really know what to do with the net.

CJ – some tools work different. When it is an input it will generate a test. When it is an output it won't generate a test.

Adam C – If you know a linkage input you can do some connectivity testing. If you didn't know if it was an input you wouldn't be able to test at all.

CJ – Linkage out would still need some interpretation. But a linkage input would allow the test to be automatically generated.

CJ – This would help increase the fault coverage.

Ken – linkage could be used for true power and analog signals or you can describe the IO nature of the pin and not put in Boundaryscan. Industry has already dealt with this by issuing warnings. May be we clarify in standard and allow in/out listed on pin.

CJ – sounds like we are back to relaxing rules on input. Not direction we should go. Could allow sloppier BSDL's to be made.

c. No Connects for different packaging same die

CJ – pin map is where we could handle the no connects rather than in the port. Syntax would be a “no connect” keyword. And would allow you to support multiple packages

Seems there is a lot of effort going on to take pins and changing them to internal to make smaller packages.

Standard doesn't allow multiple pins for a signal.

Francisco – Pin map approach may work. Final BSDL will not have needed to use Internal?

CJ – boundary register would stay the same. No need to call the signal internal. Any signal associated with NC would not cause error in tools. NC Pin would tell us that it is not bonded out. No need for engineer to convert boundary register to internal.

Bondout is only difference in part map. Signals on die still exist. Just not bonded out.

Francisco – would save time to do it through Pin Map.

CJ – multiple pin maps but smaller pin maps is subset of larger pin map and can easily be cut and pasted

Ken – Section b.8.7.1 . NC can be reserved word.

Don't want to break existing BSDL. NC could be a pin name. might want to come up with something that was syntactically illegal so it wasn't used previously. Maybe use a star *

CJ – Pin map with NC is hard to find.

Ken – Could occur in a non-English company that doesn't fully understand English

CJ – NC is negotiable. * is not a convention that many are familiar with.

Francisco – need identifier in Pin Map.

Ken - * in Pin Map. JTAG pins should not be allowed to be bonded out.

CJ – Pin map is better than port because it gives you the ability to read the conformance statement and that will tell you the which version of the standard before getting to the pin map. With new version of standard you could know that NC would not be allowed for a pin name but for multiple packages. Prior BSDLs with conformance statement before 2010 would parse the same way. Only do check against new version of standard.

Francisco – Chip manufacture may want to hide pins on different boundouts.

Ken – Agrees that Pin Map is a good choice to do it.

Ken – don't know that a pin TDI is a TDI pin in the pin map. Will have to error out further down the BSDL if TDI is called a NC

CJ – look at the name of No Connect offline

Call for new business at 112:10am EST

No new business

Meeting officially adjourned at 12:11 EST.

Next Meeting: Tuesday, Dec 15 11:00 am EST

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam to add comment about TRST. Update figure 6.8
- Comment #3 Adam will update language for any proposed change for this section.