1149.1 Working Group Meeting Minutes. December 15, 2009

Attendees:

Adam Ley
Wim Driessen
Ken Parker
Heiko Ehrenberg
Bill Tuthill
CJ Clark
Francisco Russi

Agenda:

WG membership team building
Q&A on proposed items – Let's close any open questions
Schedule for the Holidays
Call for New Business

Minutes:

Meeting Called to order at 11:04am EST

1. WG Membership Team Building

CJ -Meetings should be fun and informative. Perhaps these meetings have become a bit contentious which has not been the intention. The current Standard has room to be tweaked and should not be treated as a sacred document and is open to change. Let's restart the Working Group in a Positive manner.

CJ – Let's not look at the BSDL as a fixed thing. Software and tools evolve and change. Let's not make changes for the sake of making changes, but if there is an improvement than lets investigate it and see if it makes sense. Many vendors would support changes to make tools better

Heiko – Likes defining a list as Adam L suggested. Feels that each person should take on a task

Ken – agrees

CJ – OK if everyone is participating. Don't want it to be a blocking factor. Doesn't want to wait until all documentation is provided until items are addressed.

Already have the items that we are going to work on. Is there still concern of what is on the list that we have already?

Adam L – Spirit of his proposal was to be a low burden. A handful of sentences to describe the problem and possible solution

Ken – would like to see a living document that had revisions. All visible on the web.

Current agenda is only a few sentences long. Doesn't show what the state of the list is or who is going to champion each task.

2. **Q&A on proposed items**

Discussion goes towards the problem of capturing the correct value of two low-voltage pins shorted together (Intel's problem)

Ken- Need JJ from Intel.to discuss problem

CJ - not a problem unique to Intel. Problem exists in FPGA's. Intellitech has seen this with FPGAs with low voltage I/O. Do not think this problem is as exactly has Dave and JJ have described it and there may be other factors involved causing the error.

Discussion now goes towards NC issue.

CJ - NC is solution to pin mapping. Everything needs to be 1 to 1

Ken – Power and Grounds are exception that don't need to be 1 to 1

CJ – if you have NC, when compiled unused boundary registers does not need to be labeled as an internal and can be left as its original nature.

Francisco – Die Bond as an attribute. May give more control. Maybe if we have rules for Die Bond we can describe the unused boundary scan register better.

CJ – Solving problem with NC. This would be a minimal impact to tools. From a tools perspective DIE and Package are not different.

Ken – it would be good to display our list of items to discuss and go through them and assign individual champions to each issue.

CJ presented his list of WG items.

Observe only. – Ken

Ken – benefits not written down. Who would be champion?

CJ – chair and editor. Need to make changes in draft.

Ken – Compliance enable should have observe only (Heiko)

Adam Cron was editor of .4/ Ken was editor of .6

Look at issues in .4/.6 and why it pointed to .1

CJ – has handle on fixes that need to be made. CJ will make change to standard.

Ken – might be better productivity wise for someone to write down what the issue is and why it is important and what the solutions are. Ken will champion the Observe Only issue.

Directionality linkage. - CJ

CJ will champion this.

Ken doesn't feel he understands problem well enough to champion this. Not passionate about this Item.

Adam L – Will need to present concepts to balloting groups. Words will need to be put down on paper in a digestible format

CJ – just wants to move forward to make a motion on items for inclusion or discontinuance of an item. Wants each item to gel and allow to be present to the Working Group and to be voted on.

Power Pins. - Heiko

Is there value in identifying which pins are power and ground.

Pairing power pins with functional I/O - CJ

Separate power banks for I/O. This is seen in FPGAs but also other devices. Is there value in tying these two items together for better diagnostics?

Ken – solution is already mapped out but is may not be practical.
Can you find out the information needed to provide this link?
CJ – information can be in BSDL extension. Make it an informative part of the standard.
Ken – proposed syntax for BSDL extension. Would IC vendor document it and know how the package (power and grounds) are laid out.

Sample / Capture. - Carol
Setting a fixed 1, 0, or X.
Some pins the captured value does not have a valid meaning if pins are not initialized.
Freescale will champion this. (Carol)

TRST included in PCB level diagram. – Adam L.
Editorial issue – add picture to standard.
Do we wan to relax internal pull up on TRST?

Slow to Fall/Rise signaling issue – CJ
Compliance patterns cannot be generated for weak1/weak0/pull1/pull0 without inserting long waits for pins which may have slow fall/rise

"No Connect" – CJ and Francisco .
Need to simplify support of multiple packages with better way than defining unbonded pins as "internal"

Device ID – Still needs work
Multiple Device ID in a BSDL
Should there be only one Device ID per BSDL ?
Difficulty in making compliance patterns. Which Device ID do you pick?
This is a board level problem and shouldn't be solved in BSDL.

Low-Voltage self observe shorts coverage problem – JJ & Intel
Need to understand voltage and resistance of pin in order to identify if shorts covered or not. Input with c-s flow will capture prior to output driver Rs and Rr resistance.

Init – Carol & Carl

CJ – Is this updated document closer to what Adam wants to see.
Adam L – Yes, Closer definitely.

When will next meeting be? Decided that it will be on the 5th of January 2010.

Call for new business at 12:12am EST
No new business

Meeting adjourned at 12:12 EST.
Next Meeting: Tuesday, Jan 5 11:00 am EST

Current Issues listed and who will champion that issue.

1 Observe only. – Ken
3. Directionality linkage. - CJ
4. Power Pins. - Heiko
5. Pairing power pins with functional I/O - CJ
6. Sample / Capture. – Carol (Freescale)
7. TRST included in PCB level diagram. – Adam L.
8. Slow to Fall/Rise signaling issue – CJ
9. "No Connect" – CJ and Francisco.
10. Device ID – Still needs work
11. Low-Voltage self observe shorts coverage problem – JJ & Intel
12. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam to add comment about TRST. Update figure 6.8
- Comment #3 Adam will update language for any proposed change for this section.