1149.1 Working Group Meeting Minutes. February 9th, 2010

Attendees: CJ Clark, Bill Tuthill, Adam Cron, Carol Pyron, Adam Ley, Dave Dubberke, Wim Driessen, Roland Latvala, Ken Parker, Heiko Ehrenberg, Francisco Russi,

Missing with pre-excuse: Carl Barnhart

Agenda:
11:00AM
        Vote on motions.
                Motion to Adopt "*" to support No Connect pins
                Motion to adopt "what not to do" figure for TRST*

11:15AM
        2)   Ken -- OO on I/O pins
11:30AM
        3)   Carol - Constant Values for Sample
11:40AM
        4)   Feedback on current draft changes
11:55AM
        5)   New Business (if any)

Minutes:
        Meeting Called to order at 11:04 am EST

        Motion - to adopt "*" to support No Connect Pins
         Carol Seconded
        Vote :
        8 for
        0 opposed
        Motion passes
        * Heiko and Francisco arrived after motion passed

        Motion - to adopt the 'what not to do' figure for TRST*
        Discussion :
        CJ - has changed wording to add wording as Bus Master Connector
        Test equipment does not always have access to the node, for instance in the field, and that node needs to be toggled.
        Adam lL– key point is conditioning is not strictly a test issue. Necessary to insure that the tap controller takes on Test Logic Reset state.
        Ken – Signal is not controllable by bus master.
        CJ – if there was an embedded bus master part of power up it could toggle TRST*

Adam L – Voting such a figure should take place and details of figure are subject for further debate.

CJ – that was the original intent. might be able to expand the figure. But for now let's vote on if we need the figure and then discuss the details.

Motion - to adopt the 'what not to do' figure for TRST*
Carol Seconded
10 – for
0 – against
Motion passes unanimously

Observe Only discussion

Ken – Carl sees this as 2 tasks.

1) Go through the post section 11.5 and annex b and rationalize the terminology. This is a clean up issue.

2) Decide which classes of pins that we recommend have OO. Allow OO on a number of other classes of pins.

CJ – section 11.4.1 is telling people where they can't provide a BS pin. The Standard shouldn't try to predict the future and prevent the OO on any pins. OO can be on compliance enable and non digital pins.

Adam L – would submit they could also be TAP pins.

Carol – being on TAP pins will cause timing issues.

Ken – or what it would be useful for?

Adam L – sees no reason to preclude it in the standard.

CJ – would hate to send people down a path where no one would get benefit from putting Observe Only on TAP signals. But don't want to predict the future.

CJ – the input is noted and the group will need to think it out more

Adam L – Rule C is a prohibition against cells that have a controlling function.

CJ – Can add back 2 and 3 and redefine the wording.

Section G wording could include TAP pins. Wording will probably need another go around.

CJ – 1149.6 is the better standard than 1149.4 for testing differential pairs.

Will add figure for differential with Observe Only.

Carol – ok to allow it but may be problematic, may cause signal integrity problems if used.

CJ – known and understood. That is what you need in 1149.6. Just trying to show it and allow it.

Ken – **Rule E is a permission with the "may"**
CJ – will need to reorder these.
Ken – need to be careful with cross references.

CJ – **R needs to be a permission rather than rule**
Adam C – "Observe Only" needs to be bold like "linkage"
.

Ken – Note that goes with t looks like a permission as well

Wim – would like output pin expected state value to be available when generating an automatic test for that pin.

CJ – not that there should be an expected value. Mixing permission to have object only and generating pattern for ATPG

Ken – example of what Wim is referring to is if a monitor that is looking for 1v supply would it interpret the 1v as a 1 or a 0.

Wim – only the designer would know this. This information should be placed in BSDL

CJ – These pins would be in the class of pins that you can not predict the value on the pin.

Carol – would be difficult to document behavior of OO under all conditions.

Wim – having the OO would be good to know if a power pin was disconnected or connected to ground

CJ – trying to avoid a future problem like we did with .6. Want to prevent future standards from being non compatible with .1 because we were overly restrictive

CJ – want to allow Observe Only where possible and not be restrictive.

Ken – Internal cells. Function field and boundary register are always internal

Adam L – function is Observe Only.

CJ – these are the given functions, Control, Observe Only ,etc

CJ –will possibly redo figure B.8 to show more/better descriptions for Observe Only.

Carol – Constant Values for Sample.

High level rational as to why we do this.

With all the complexity and multiple configurations requirement for sample to always operate correctly in mission mode is difficult to support.

Demands of low power designs that require power saving modes. Power down selective inputs before there is a driver to the boundary register cell. BS Cell is blocked by power saving circuit. Would need to power up path to sample data.

Power up sequence may be long and may not be able to get around to do sample

Security Aware chips. Mission mode operations when security is in action, SAMPLE mode is restrained to Boundary Scan register.

Leave as a STRONG recommendation to have SAMPLE the way it has been traditionally. Many chips don't have compliant SAMPLE and don't admit it.

Ken – Reasonable points. The world has changed. Interaction between Sample and Mission mode are more complicated now

Adam L – Very purpose of SAMPLE is to acquire information about the mission mode of the chip that isn't usually assessable. Using an X as the expected will give you a carte blanch for not having SAMPLE return real data

Ken – Restrict change to stating that SAMPLE is declared X. Make best effort to get data but can't predict what it is going to be.

Adam L – they way Sample is already defined. Going to capture at the primary IO

Carol – The way SAMPLE is used is , taking a sample of pins. Data changing at higher rate than TCK. Not sure what the data is anyway. Take several snapshots to try and determine data.

Adam L – can halt system before using SAMPLE

Carol – No expected data and just look at data ?

Adam L – want people who misuse SAMPLE to have to write Errata or admit to SAMPLE not being compliant

Ken – need to offer people more guidance as to what SAMPLE means

Adam C – Adding OO cells. Could add on control signal that power downs the pins and use that to know that the pins are powered down and can SAMPLE.

CJ – proponent of Sample. Not sure where the problems are coming from.
All we want to do is register value into BS cell

Carol – what you think you may be getting may not be what is going in to Cell due to complexity of circuit(power down, security)

Adam L – Fundamental misunderstanding is that SAMPLE requires that you capture the state of the Pin. As far as the Cell descriptors go the capture values are purely related to the BS Cell itself. Fan in multiplexer that takes in several inputs and selects one for capturing in the Scan Cell. That is all the descriptors tell you. Where does that wire come from.

Adam C – do you have same logic in Extest that

Carol – Branch off to Boundary register. Want to truncate the path and make it a training stub load. Whole path is removed in mission mode.

Adam C – use same path for Sample that using for Extest.

Carol – interrupted Mission Mode. Signal integrity will be disrupted.

Roland – distinction in .6 mission receiver

CJ – do the same as when you are in SAMPLE when instruction is loaded.

Carol – two choices allow sample to capture non valid value or interrupt mission mode

CJ – can we look at FPGA's? Have full bi direction cells on configurable pins. (I/O's can be programmed a lot of different ways)

Carol – because FPGA's have already set themselves up

Carol – before programming FPGA do you do a SAMPLE that is meaningful?

CJ – no because you wouldn't be looking for anything. IO not programmed. If IO are not INIT'd than your IO's are not properly configured.

Adam C – After you program can you do SAMPLE?

CJ – yes.

CJ – Many devices out there are managing SAMPLE on critical signals. FPGA's have high speed data busses like DDR3

Carol – biggest problem on Gigabit serial pins. Mission receiver will not correctly get data if SAMPLE is turned on during mission mode.

Adam C – issue is that when you turn SAMPLE on, the mission mode receiver doesn't work correctly due to SAMPLE logic being in the way.

Carol – correct it doesn't work at 3 Gigahertz

Ken – SAMPLE doesn't fully work today and needs to come up with new meaning for today's circuit

CJ – what we might do is change the wording of SAMPLE to make SAMPLE look more like EXTEST mode?

Carol – they are identical

Adam L – could care less in mission mode what the test receivers capture.. it could capture X. Somewhere the state of those signals in mission mode can be sampled. Need a 3rd cell that captures the logic output of the mission receiver.

CJ – for differentials signals the requirement would be that the single end of the receiver have SAMPLE. But relax Observe Only on the differential receiver.

Carol – that is ok for differential receivers, but not for the power down pins.

CJ – people are not looking to capture values on powered down IO's and expecting to see something there. Not concerned during the power down state.

Carol – how do we specify that in the BSDL that it is allowed.

Carol – standard says that if you put a logic 1 on the pin you should get a 1 at SAMPLE. This is not the case when IO's powered down.

Adam L – this is a gray area that could use stronger definition.

CJ – standard isn't expecting values on powered down pins. Need to make that area more clear in the standard.

Carol – the last example, security impacts designs in many way. Hackers can use SAMPLE to see what is going on inside the chip. EXTEST will wipe all secure information so that is different.

CJ – SAMPLE doesn't give any more information that than removing chip and using a socket.

Carol – SAMPLE makes it easier for the hacker to grab data.

CJ – still not reason to remove SAMPLE for IO. Many other ways to get data as well such as socketed part, traces on outer layers, logic analyzers.

Carol – these other methods requires more sophistication for a hacker.

CJ – not so.. can get used equipment for low $$ easy to set up logic analyzer/scope

Carol – SAMPLE is supposed to be non intrusive to mission mode. This is problematic to designers.

CJ – can make clarifications on differentials and power down to help.

Carol – suspects that there are other cases than just differentials and power down that will arise.

Carol – SAMPLE is expensive to industry. Is it worth the cost??

CJ – need to look at spec to make it clearer for designs. Look for places to back down in spec where it makes sense.

Carol – such as not be disruptive to high frequencies?

Meeting adjourned at 12:17 EST.

Action item for everyone – take a look at changes (text and figures) to draft and see if there are any concerns.

Next Meeting: February 16th 2010 11:00am EST

Current Issues listed and who will champion that issue.
1   Observe only. –   Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:
- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.