1149.1 Working Group Meeting Minutes. March 23rd, 2010

Attendees:, Carl Barnhart, Adam Ley, CJ Clark, Bill Tuthill, Carol Pyron, Roland Latvala, Heiko Ehrenberg, Ken Parker , Wim Driessen, Dave Dubberke, Francisco Russi, Adam Cron

Missing with pre-excuse:

Missing: Bill Eklow,

Agenda:
Discuss the draft and clear up any misunderstandings

Minutes:

Observe Only

Carl – is comfortable that OO can be on any pin.. What he is not comfortable with are the rules are not clear and results are not absolutely not clear. Doesn't see a way to code the tests to use this. Changes made to standard make a debug tool not a standards tool. No way to communicate to designers the definition of what the standard is.
Point of standard is to define restriction and constraints to allow all vendors to work inter operability. Not there yet.
If we provided a mechanism for OO that shows the expected value. Then we could relax some rules
Short of clearly defining the constraints and clearly stating the expected results we don't have a standardized capability.
CJ – Standard is a device level standard. Not standardizing so tools have interoperability. Not part of our objective.
Have definitions of how instructions look right.. Don't innumerate all possibilities of instructions. Let end user define that. Don't define the length. Let the chip designer implement that. Same with OO on any pin. Just because we don't specify exactly how it is done on a power pin doesn't make this a standard
Carl – what is the problem the with adding an expected value field
CJ – compliance enable if it is set to a 1 or a 0 can predict what the value is.
Carl – how do you communicate to the ATPG tool what the failure case is.
Roland – gave some information on how to do this
Carl – no such equivalent for power or analog pin. Cant easily predict what the expected value is
CJ – only define capture values in BSDL. Only place for expected values in the standard.
Carl- rules that there are no inversion.. 1 into a driving cell and receive a 1 in good machine case.
Carl – need to add expected value to BSDL. Need to supply what good machine value is.
CJ – See what the group has to say.
CJ – OO cells are no different than any other cell. Chip level design standard. Allow OO on any pins. Other than tap pins.

CJ – asks Francisco if he is comfortable with OO on any pins

Francisco – in favor of it

Adam L – mischaracterized Carl's argument. Carl isn't all together at odds on any pins. His concern is (which is valued) what are you actually observing and how is that encoded into a valid binary value. Suggestion that 1149.1 doesn't address concern for ATPG is preposterous.

Wim – in favor in OO pin. Likes the idea of knowing what is on the pin. Should make rules that power/ground/ cells 1 is pass 0 is fail

CJ – fail monitor concept

Ken P – agrees with Carl. Adding a lot of cells to the BS register is large. "Willy-Nilly" addition of cells for dubious test value is encouraging bad behavior. If there is no clear cut advantage to do something we shouldn't

Adam L – idea of BS cells being added "Willy-Nilly" is preposterous. Adding boundary cells at defined ports of package is finite in number. Idea of OO is to take a BS cell and associated with a port. Agrees with Carl and Ken that if you can't make sense out of it than it has no value. Should define a way to make that value add achieved. Example. Power pin. Might have some portion of chip that power isn't required under certain conditions. To say 1 is passing or 0 failing doesn't make sense. Want to know if power is available.

Carl – need to state what OO means on a power pin. Doesn't know what it means. Need to exempt some pins from existing boundary scan rules.

Carl – rules on a pin are meaningless unless we know what the good value is

Adam L – Rules that are currently defined are defined for capturing digital values. If we want OO on power pins we need to define a new set of rules for non digital pins. Idea of OO on every pin is simple and elegant but also complex because it is not considered in standard

CJ – neutral party but capturing momentum in working group. Result of that momentum. Not sure where inversion of logic comes into play.

Adam c – a negative value on power in.. What is it captured as?

CJ – depends on what is defined as good.

Carl - how do you communicate that to the world?

Adam L – BSDL defines values for ATPG

Carol – edit is not sufficient. Need to take off 2 cases of clause c. new rules for power/analog pins on OO should provide an expected value of what is a passing condition.

CJ – we agree on the removal of item 3

Carl – agree that is what we want.

Carol - #3 is causing the most problem. And change compliance pins has optional OO cell.

Francisco – sees this as important for users in the future to have OO for debugging. Feels it is valid to have OO on power pins.

Carl – volunteers to make changes to the OO rules to meet his objections. Will take at least a week to come back with some changes.

Ken – all can imagine how an OO on a compliance enable can be utilized. Power / ground/ analog pins are what are causing the issues. Practicality problem in detecting open on power pins which is what the OO is needed for.

CJ – no one really has a way to do this with the power pin. More of a permission to allow. If Momentum of WG has changed would rather do away with it.
Carl – feels OO is worth doing and elegant. It has consequences though. If we are going to add to boundary registers, there are a lot of rules for boundary registers to follow. Need a way to let the world know what the good machine value is on none traditional cells.
Carl – would like to table topic while we work out details
CJ – we(the working group) are just talking about section c3 being the problem. We are comfortable with removal c2?
Carol – comfortable with removing C2 if add "optional" attribute somewhere else.
Carl – agrees that c2 could be removed.
CJ – c3 seems iffy. Carl will look into this in more detail.
Carl – standard is defining behavioral rules.
Adam C – get a second source you know what the rules are.
CJ – you can get different results
Adam c – you can drive a 1 on one chip and 1 on another and two different correct values?
CJ – no
Carl – table topic and pick it up when we get more information

Power/Linkage pins

Carl – doesn't care what we call them.
Ken – linkage is pure VHDL word and decided to move away with compatibility with VHDL.
Carl – would need to remove links that say subset of VHDL
Carol – appropriate to make that distinction but ok to move away from VHDL
Carol – the idea of the different linkage key words is to remove linkage.
CJ – missing GROUND in draft as well as LINKAGE_MECHANICAL will add.
Carl – is POWER_NEG a ground?
CJ – POWER_NEG is any power that has potential less than zero
CJ – GROUND is on list in standard only need to add LINKAGE_MECHANICAL.
Carol – not sure how to incorporate current linkage pins.   Have temp sensor pins
Carl – is it an analog in?
Ken – It is an analog out.   This would be just a LINKAGE_OUT since it is transmitting some analog value out
Carol – wasn't worried about what to call a pin before because we had LINKAGE_OTHER as an option.
CJ – don't want LINKAGE_OTHER to be a catch all like the current "Linkage" usage
Carol – how would you treat VREF. Is that POWER_POS? LINKAGE_IN? This is a termination voltage for DDR
CJ – POWER_POS
Carl – this is a case where OO makes sense. Not a ganged power pin.
Adam L – VREF is a mid rail voltage. It defines how 0 and 1's are defined
Adam L – nice to have an OO but still have issue of what captured value means.

Carol – Is happy with names. Only concern is not having LINKAGE_OTHER. Need LINKAGE_MECHANICAL.

CJ – sense was that LINKAGE_OTHER was not a good idea and could lead down the same path as current linkage keyword.

Carol – from the chip design point of view we have a lot of "weird" pins. Sometimes we don't want any one to know about some pins and don't want them touched. These are usually NC pins though. May not want to describe all pins in the BSDL

Roland. What is LINKAGE_BUFFER for?

CJ – this was added due to request by Roland. Mirroring what we have in the digital side. Outs are 3 states. Buffers are 2 states.

CJ – there is very little use for buffer.

Meeting adjourned at 12:02 EST.

Next Meeting: March 30th 2010 11:00am EST

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.
1   Observe only. –   Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:
- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.