Date - 07/01/2011

Minutes of the IEEE-1149.1 Working Group Friday meeting

Attendees:

Adam Ley,

Brian Turmelle,

Carol Pyron,

Craig Stephan,

Roland Latvala,

Carl Barnhart,

CJ Clark,

Francisco Russi,

John Braden,

Dave Dubberke,

Peter Elias,

Ted Eaton

Excused:

Ken Parker, Wim Driessen, Heiko Ehrenberg

Meeting called to order at 8:35 am MST

New Draft: P1149 1 Draft 20110617.pdf (clean.pdf)

Agenda/Overview:

REGISTER_MNEMONICS and REGISTER_FIELDS flattened examples REGISTER ASSEMBLY and PREFIX discussions

Minutes:

During the first part of the meeting today Carl presented examples of REGISTER_MNEMONICS and REGISTER_FIELDS for flattened case in BSDL

REGISTER_MNEMONICS example review

- Mnemonic group names are VHDL identifiers
- % symbol is allowed in mnemonic names
- 1.8V allowed since not a number
- Bit values can be 0 1 X only
- <> symbols are 'less than and greater than' and in fact not chevrons or angle brackets per Carl's research, but current wording in the doc will not be changed again.

REGISTER_FIELDS example review

• Flat initi_data example only, hierarchy has been moved to REGISTER_ASSEMBLY.

- Bits are allowed to be used more than once, but tools should flag this as a warning
- It was discussed that no commas are required before the NOPI NOPO NOUPD keywords to improve readability. The WG all agreed on this.
- If a full register then bits can be sparse (REGISTER_ACCESS defines total length)
- If a register segment then all bits need to be defined for later assembly
- The length of each register or segment will be defined within square brackets [] after the name of the field. Example init_data [180]
- Carl to talk to CJ about more complete definitions for IREAD, IWRITE, SAFE, and IRESET keywords relative to NOPI NOPO NOUPD usage
- CJ discussed this somewhat in the meeting too. Basically the BSDL defines the static structural behavior of the register cells for static predictions. PDL will allow for dynamic predictions based on context of an operation. Eg: If you have NOPI and due a shift operation the shifted value will come back since there is no capture to overwrite it.
- CJ discussed IRESET behavior and the subtleties of NOUPD. It is assumed the
 reset is on the update flop, but possibly the capture flop too if both are present.
 However there is no easy way for a tool to predict this, or if the update stage gets
 captured back into the capture shift stage, so unlikely tools will make predictions
 of the captured state during IRESET.
- Carol inquired if there is an order for IRESET, IWRITE, IREAD, NOPI, NOPO, NOUPD. Carl responded No, but only once instance of each is allowed for a given register field.
- Adam asked Carl to fix syntax in the bit ranges in this example which were overlooked

In the last 25 minutes CJ then lead continued discussions on REGISTER_ASSEMBLY and PREFIX usage.

REGISTER ASSEMBLY

- CJ asked about ARRAY usage in register assembly and said it would make coding better for compilers.
- Carl said you are allowed to use ARRAY in a string in VHDL
- Peter was ok with using ARRAY as CJ requested
- CJ took action item to further develop the syntax of register assembly

PREFIX

- CJ showed usage of PREFIX based on Francisco's prior STIL scan chain definition
- CJ built on Peter's example and split the hierarchy into segements: PREFIX 1, PREFIX 2 and PREFIX 3 for reuse and readability
- Peter commented that although this was intended for machine use, the human interface cannot be overlooked since that is where we engineers get involved during debug and correcting mistakes and errors.

- Carol asked if we are defining verilog hierarchy and noted that delimiters can be other characters besides period (.).
- CJ responded that PDL uses the (.) and we are looking at scan chain definitions for BSDL and want to make readable. This is a sanitized version of the scan chain report for PDL and BSDL use.
- Carl commented that P1687 may want to take advantage of this convention for iScope. CJ agreed this may be useful format for them.

Meeting adjourned: 10:05am MST

Action Items:

- Carol to add supplemental BSDL examples based on Carl's current draft.
- CJ continuing with REGISTER_ASSEMBLY definition and will update the parser.

Next Friday Meeting:

• Next week Friday July 8, 2011