Date – 06/10/2011

Minutes of the IEEE-1149.1 Working Group Friday meeting

Attendees:
Brian Turmelle,
Carol Pyron,
Craig Stephan,
Roland Latvala,
Carl Barnhart,
CJ Clark,
Francisco Russi,
John Braden,
Dave Dubberke,
Ken Parker
Wim Driessen

Excused:
Adam Ley
Heiko Ehrenberg

Meeting called to order at 8:30 am MST

New Draft: P1149 1 Draft 20110528.pdf (_clean.pdf)

Agenda/Overview:
- CJ lead another working session on Register Fields

Minutes:

CJ raised the question of REGISTER_FIELDS pin association description:
- It was agreed that register fields association description should only be for chip level per B.8.1.1
- Register fields association will not be required in package files for IP subblocks in B.10.1.1

Ken asked what REGISTER_ASSEMBLY attribute was for.
- CJ/Carl explained it was to be used as an alternative or in conjunction with REGISTER_FIELDS to concatentate package files. One nice feature of this is that you wouldn't have to define the total length of the register. The tool would determine the length from the sum total of bits it assembles.
- Carol confirmed that the order in the BSDL is important:
    - Register Mnemonics
    - Register Fields
    - Then Register Assembly

From the test case CJ sent out this week the discussion of reserved Keywords came up.

- It was agreed that we would respect BSDL keywords (like CLOCK), and that nobody wants to change this now. The same keywords should be in each version of the Std.

Ken raised another question about how much of the fancier super-structure of 1149.1 2011 do we want to carry in the BSDL? Specific protocols for internals of a chip do not apply to simple EXTEST. This opened a discussion lead by CJ on the importance of the new features and how that they should all be supported in BSDL and 1149.1.

- Carol mentioned this was lead by the Dot6 initiative to have the Init-data register and mnemonics for its electrical properties of IO's tied to specific industry protocols (xaui, pex,sata, and so on)
- CJ explained that P1687 does not address the board test issues and TDRs.
- John described a monster chip with 25K C4 balls, and 4000 C4 package balls. And that this complexity needs to be managed by the Std going forward.
- Ken doesn't want to see 25,000 lines of BSDL. The more complex the more likely vendors will deliver bad BSDLs.
- Wim wants to see concise interfaces defined in the BSDL/PDL at the chip level. He has concern about IC vendors delivering PDL for the IP sub-block that does not map to the IC Chip level interface cleanly.
- Wim also stated that any register defined in PDL should be defined in BSDL and translate to chip level IO pins. A PDL for an IP which has a PDL for sub-block information is more than he wats to see.
- CJ explained that if you only need EXTEST capability then you can ignore everything in the BSDL that is not related to the Boundary Register and Init_Data Register.
- Carl mentioned there could be board level PDL and chip tester level PDL. CJ disagreed with this and stressed the reused on IC tests at the Board level in the field. The emphasis on reducing test costs and reducing customer returns across the industry. The hooks we are putting in place will help facilitate this goal.
- Carol polled the WG to see if we are all on board to proceed with completing our current BSDL/PDL objectives. The vote was unanimous YES to proceed.
- CJ set the expectation of late July to finish the work.
- Carol agreed the Body, and Annex B,C are done. Need to finish up the BSDL. CJ to continue his work and Carol to provide an updated BSDL example with the latest enhancements per Carl's latest draft.

Meeting adjourned: 10:00am MST

Action Items:

- CJ to continue REGISTER_FIELDS work.
- Carol to update the BSDL example.
- WG members to continue to review and provide feedback to Carl.

Next Friday Meeting:

- Next week Friday June 17, 2011