Date – 02/11/2011

Attendees:
Carl Barnhart,
CJ Clark,
Dave Dubberke,
Ken Parker,
John Braden,
Brian Turmelle,
Carol Pyron,
Roland Latvala,
Francisco Russi,
Ted Eaton,
Mike Ricchetti

Agenda:

1) Review of latest IC_Reset rules in Carl's strawman document (Document4)

Meeting Called to order at 9:30 am MST

Minutes:

Overview: Carl presented latest draft of IC_Reset rules. He will begin importing IC_Reset rules into the main document this coming week.

Today's discussion points:

IC_Reset Rules:

- Carl started with a review of the diff document from prior changes
- Recommendation - rule g.:
  - CJ asked for an editor's note about blocking exernal reset pins and also internal reset domains.
  - The rule g, text was reworded to add clarification
- Recommendation - rule h.:
  - Is a companion to rule g.
  - CJ thought a note on granularity might help rule h.
- John/Carol/CJ agreed with Carl's new wording of rule g. 'pin or internal source'

IC_Reset Permissions:

- Carl started permission section hadn't changed in this draft.

IC_Reset Description:

- Carl reworded with input from Dave and Ken this past week
- Block of text removed

- Carl to rework again to match the rule g above. Rules g. and h. are recommendations not strict rules.

Reset-Select Register: (figure ??1)

- Carl - Asked CJ to remove text blocks from figures.
- Ken - Stated this is a non-standard drawing, which hasn't appeared before.
- Carl – The dotted box has been placed around the reset-hold bit update stage again. Capture and Update are both test logic.
- CJ - Asked if anyone objected to treating the update flop as mission logic.
- Carol – Update stage is resettable by TRST* so is ok with it.

Reset-Select Rules:

- Carl – One pair of A/B bits per reset domain.
- Rule i.)
    - CJ - New – Document in BSDL register fields and port associations which external reset pin the A/B bits correspond to.
    - Carol – Port associations must be optional
    - CJ – optional only if no pin, but mandatory if there is an associated external pin
    - CJ – from tool prospective the port association should not be optional for diagnosis
    - Ken – recommended test to describe the port associations
    - CJ – PRBS tools could figure out the pins from port associations
    - Carl – Added new text – Use reg fields and where reset source is an external pin then also use port association
    - John – ok
    - CJ – ok
- Rule j.)
    - Carl – should bit polarity be required to be specified?
    - Carol – No
    - CJ – Not a big fan of letting designers do what they want. Should define the polarity of the 'safe' value
    - Carol – What about pll lock ratios – no default exists
    - CJ – Designers should use init-data register not reset-select register for that.
    - Carl – Note rule h.) describes TDI = 1, should there be a rule about TDI safe value not being allowed to cause any damage?
    - Carl – The rules currently only define the 3bits A,B,C individually, nothing about floating TDI safe values.
    - CJ – Carol we are encouraging people to put the extra 'C bits' into a separate register. Keep reset-select register dedicated to the reset functions only.
    - Carol – Custom bits could be needed for lots of reasons. Security, Boot, Fuses, Repair, etc…
    - Carl – Maybe we remove the 'C bit' completely from this register.
    - CJ – I want something in between these two positions. eg: Use the C bit for selecting core1 or core2 reset domains.

- Carol – Taking Ted's earlier position, asserting resets alone may not be very interesting. Modifier bits are needed to control state machines, and other actions.
- Carl – Other actions how?
- Carol – Quantifiable. Reset action, post reset actions.
- CJ – Use other tdrs for the post reset actions.
- Carol – OK then – Take out the custom C bits
- CJ – Low hanging fruit ok, but want to avoid feature creep.
    - We want IC_Reset to mimic the reset pin being toggled
    - Its too far when we want it to do everything
    - Better to issue a private instruction for the fancy stuff the issue IC_Reset to operate on it.
- Ken – Simplicity may be better than complexity.
    - Are you saying IC_Reset may not work if some Security key has not been run yet?
- CJ – No! The external reset pin will still get asserted.
- Carol – To clarify a security key is needed to go beyond a certain point
- CJ – Extra C bits all need to go to 1. Designers will need to use other registers to set misc bits to other vaules. Fancy functions would be tricky to implement in this register. Bit C should be simple usage. Reset core1 or core2 but perhaps not both as defined by the user.
- Carl – CJ you are still stuck on the one reset-enable/control per pin source. Each source has its own 2 bit A/B pair. Bit C is not required.
- CJ – Ok then in terms of the Std, 2 bits per source if multiple domains.
- Ken – I want to understand – 2 IC's each have a reset pin. One designer uses a single reset domain, the other uses 20 internal reset deomains. Who is correct, or both ok?
- Carl – That doesn't make sense.
- Ted – That makes perfect sense.
    - Master reset
    - Local resets of each subdomain
- Carl – ok then.
- CJ – At a minimum the pin would have it's A/B bit pair, and optionally internal reset subdomains.
- CJ – We can get rid of the 'C bit' from this register then.
- Ted – Are there then no extra bits in this register? I will loose test persistence.
- Carol – You'd have to use another instruction to set the extra bits
- Carl – Don't bring TLR to those tdr registers.
- Ted – These registers get a reset from TLR.
- Carol – Could we add 'TLR blocking bits' to block TLR to specific registers inside the reset-select register? Ted's position makes sense.
- Carol – Give these bits a very regulated purpose in life.
- CJ – could use a many reset pairs as you like. Nothing to dictate implementation.
- Carol – This would be a well regulated case

- John – 'Creeping featurism' may affect acceptance.
- Carol – It may be worth while in this case.
- CJ – Let's get something done, learn from it and see what has to change. I'd be interested in a simple IC_Reset that mimics the external pins and some finer control. We should be moving quicker.
- Carl – Any objections to removing the C bit?
- Ted – Take a vote?
- Francisco – Allow time for objections from all 11 participants.
- Mike – Ted, how does your PLL example work?
- Ken – IC_Reset has priority over persistence.
    - Block I/Os and system reset pins, no fuctional reset will occur.
    - IC_Reset has higher priority over test persistence to reboot a board
- Ted – If we don't have the ability to block TLR to registers, then we don't have control of the entire reset system.
- Francisco – Anyone else have objections.
- CJ – Note 1 objection to removing the C bit and let's move on.
- Ken – General question: When a shared POR is used for both System POR and Tap POR will the reset-select register be isolated to the system reset side, and not affect the Tap POR?
- Carol/Mike. – Agreed the Tap POR cannot be blocked.
- CJ – Remove the C bit and also update the drawing to not allow intercepting the POR to the TAP.
- Carl – TAP POR and System POR were assumed to be separate.
- Carl – Rule f.) then needs a separation of test logic and system logic resets, or internally generated TAP POR for my internally generated reset signal to the test logic.
- CJ – POR*
- Carl – Why does polarity matter?
- CJ – Just for consistency across figures.
- Ken – For the shared POR to system and TAP, do I go south of the point where it drives the TAP reset? Never put a bit pair in series to the TAP, only to system reset pins.
- Carl – Correct. Will add to the text.
- CJ – Will add a figure and send to Carl.
- Carl – Do people want to see this draft or wait until incorporated into the main document?
- CJ – Yes, I'd like a copy.
- Carl – Lastly I've redone CJ's figure of reset-select register to remove AND/OR and replace with a MUX to simplify the drawing.

Meeting adjourned: 11:00am MST.

Action Items:

- Carl to incorporate these strawman rules into the main document..

Next Working Group Meeting:

- Next meeting Feb 18, 2011