August 20, 2010

Minutes of IEEE 1149.1 - Initialize Sub-Group Meeting

Attendees:

Carl Barnhart
CJ Clark
Dave Dubberke
Ted Eaton
Roland Latvala
Adam Ley
Ken Parker
Carol Pyron
Francisco Russi
Sivakumar
Brian Turmelle

Minutes:

This meeting continued the discussion of the new init field definitions.

- CJ raised the issue of identifiers; that in the string values of BSDL attributes we did not need to follow VHDL identifier lexicon. Carl responded that such was the practice to date, and changing that would require defining a new identifier lexicon for BSDL. It was determined that VHDL identifiers were a subset of TCL and, therefore PDL identifiers, and so should work as-is, and the issue was closed to reduce the editor's work.
- Carl started going over the latest example REGISTER_FIELDS definition.
- It was pointed out that if a bit of a register could appear in more than one field (ex: a reset field to reset the whole register, plus other fields), then there must be semantic checks to ensure that there are no conflicts in default value assignments. (In PDL, the last 'iWrite' would dominate.)
- There was lengthy discussion of the implications of allowing essentially random-ordered bits and ranges of a register to a field, and the effect on a hierarchical field. A hierarchical field can only support a "downto" range of contiguous bits for the register bit assignments.
- There was a lengthy discussion of how to build a register, and the role of bit assignments and lengths in that definition. The current scheme requires that there be a known length, and then allows subsets of that length (with bits and ranges) to be assigned to fields. Not all bits must be specified, order of specification is unimportant, and bits of a register can be assigned to a field essentially in random order (a common characteristic of synthesis stitched chains.) CJ wants to be able to build a register by simply concatenating fields, which means that the designer need not calculate specific positions within the register or even know ahead of time how long the register is. All that can be calculated. Carl agreed to see if simple modifications of the current scheme would allow this concatenation as well in a reasonably consistent BNF.

Current Status:

Formalize Rules – BNF coding in progress.

BSDL Constructs - – In progress.

Formalize PDL constructs – no activity this week

Actions:

- CK to draw TDR example(s) for hierarchical structures.
- Carl will code CJ's examples both with segments as arrays and as scalars.
- CJ will provide an example of a dynamic register for discussion.

- Carl to modify examples and BNF to conform to today's decisions, and to attempt a version for a bottom-up build.

Work still to be done:

Incorporate INIT into 1149.1 Std

Next meeting date:
Same time next Friday August 27th