Date - 01/21/2011

Attendees:

Carl Barnhart,
CJ Clark,
Dave Dubberke,
Heiko Ehrenberg,
Roland Latvala
Adam Ley,
Ken Parker,
Carol Pyron,
Mike Richetti,
Francisco Russi,
Brian Turmelle

Agenda:

1) Continue review of IC-Reset Instruction.

Meeting Called to order at 11:30 am EST

Minutes:

Meeting started with a review of the editing status.

- Carl: The body (without Annexes) is ready for posting and starting review except for the IC_RESET instruction and its reset-select register.
- Annexes have not yet been tackled, and to some degree are awaiting the BNF work to be completed.
- We should use email for discussion, changes, additions to the text, and meeting time only for voting for adoption. Carl will drive the email review.

We then continued the IC_RESET and reset-select register discussion.

- CJ: The CPC/TPC is used to hold registers needed to hold the pins constant. That does not apply to the reset-select register, and we may need to hold a reset through TLR while the pins and system logic are active so the CPC/TPC and IC_RESET need to be independent.
- Adam: 1149.7 has a system reset capability from the TAP with unknown overlap. Adam will present to the group next Friday.
- CJ: Per Ted's request for global CPC/TPC control of resets to TDRs, we already show both blocked and unblocked reset signals, and these are available for use with any user TDR.
- Carol: We are making a much greater distinction between TLR and TRST than in the past.
- CJ: It is more flexible if we retain a bit defined as allowing TLR to reset or not.
- Ken: I think Ted believes that it is too burdensome to implement the CPC/TPC in order to get TLR persistence.
- Carol: Maybe we should look at a CPC/TPC with more bits for greater control.

- Adam: Perhaps a "Persistence Controller" with multiple bits for TLR suppression, I/O clamping, user defined functions. Test reset is global and should be controlled globally.
- CJ: We could provide capability of blocking TLR, but should not mandate it, and provide TLR control locally.
- Francisco: The reset select could also be used to control and hold power domains in the powered-down state. That would need to be held through TLR.
- CJ: We could make the TLR control bit of the register optional.
- Carol: The TLR control bit makes sense.
- Ken: The picture details need to be cleaned up.
- Carol: Optional bits could have any "off" state. Use PDL and mnemonics to define.
- Carl: I disagree; loading the register with TDI at '1' must load the "safe" or "off" state (which could be '1' or '0' in the update registers.)
- CJ: Use default of all '1', user can invert as desired.
- CJ: We're running out of disagreements.
- Roland: There is a lot of overlap possible between the reset-select, init-data, and other registers. They may be shared or have shared segments.
- Mike: That is similar to what we use.
- Ken: Bit "B" of the figure has different names in the figure and the rule. The figure is missing reset pin and the logic and signals to the system logic.
- Carol: The reset-select register has higher priority than the boundary register (assuming an observe and control cell) which has higher priority than the pin.
- Carl: CLAMP behavior does not have rules for INPUT cells, only outputs.
- Ken: Should CPC/TPC have mandatory affects on INPUT boundary register cells?
- Carl: As far as the reset-select register is concerned, the behavior of the pin and boundary register are immaterial.
- Adam: No matter how we block TLR, this needs to be shown as a change to the machine.
- Carl: I think that's covered; please review Clause 6 when I get the next version of the draft posted.
- Adam: We need to document the interaction of the CPC/TPC and reset-select.
- Ken: How should we handle internally generated resets? We should use the same two-bit structure for consistency of control.
- Francisco: Also very useful for power domain and isolation controls.

Meeting adjourned: 1:00pm EST.

Action Items:

- Carl to update strawman; CJ the figures.
- Adam to present 1149.7 system reset capability.

Next Tiger Team Meeting:

• Next meeting Jan 28, 2011