Description

Reference voltages a frequently key to the operation of IC I/O. Currently there is no language in the industry that documents in a machine readable format the relationship of the reference voltages and the I/O which depend on the input voltage. Despite having INIT_SETUP, failures at the I/O can occur simply because a POWER_POS or VREF_IN voltage is not present or not turned on at the board level. Programmable devices may control DC-DC circuits and these programmable devices may not be programmed at the time test is performed. Test engineers must consult datasheets in order to understand the relationship of what power and voltage references control which particular IO pins. The datasheets sometimes are unavailable to the third party manufacturing test engineer or available only under NDA. POWER_PORT_ASSOCIATION is an attribute which collects this valuable information in one place in a machine readable format.

<power port association statement> ::= **attribute POWER_PORT_ASSOCIATION of** <entity_target> **is** <power port association string> <semicolon>

<entity_target> ::= <component name> <**colon** > **entity**

<power port association string>::= <quote> <power port association list> { <**comma** > <power port association list> } <quote>

<power port association list>::= <power port id> <**colon** > <lparen> <port assoc list> <rparen>

<power port id > ::= <VHDL identifier> | <VHDL identifier> <lparen> <decimal number> <rparen>

<port association list> ::= <port id> { <**comma** > <port id> }

```
attribute POWER_PORT_ASSOCIATION of mydev : entity is
"DDR_REF1    :     ( DDR_DATA(7), "&
"                    DDR_DATA(6), "&
"                    DDR_DATA(5), "&
"                    DDR_DATA(4), "&
"                    DDR_DATA(3), "&
"                    DDR_DATA(2), "&
"                    DDR_DATA(1), "&
"                    DDR_DATA(0) ), "&
"IO_REF1      :    (  SERDES(0), SERDES(1) ), "&
"IO_REF2      :    (  SERDES(2), SERDES(3)  )";
```

Semantic checks

a) <power port id > must be a previously defined <port id> with port type of POWER_POS, POWER_NEG, POWER_0 or VREF_IN.
b) <decimal number> must less than the size of the <port id>
c) A given <port ID> shall be previously defined in the port description.
d) If a <port ID> is a <subscripted port name>, the <subscript> (see B.6.2) shall lie within the range specified for the bit_vector of the relevant port.
e) A <port ID> may appear only once for a given <power port association list>