

Date – 8/26/2013

Attendees: (15) CJ Clark, Bill Tuthill, Brian Turmelle, Craig Stephan, Frans de Jong, Gobi, Marc Hunter, Gurgen Harutyunyan, Mike Ricchetti, Roger J. Sowada, Teresa McLaurin, Dharma Konda, Dwayne Burek, Josh Ferry, Ismed Hartanto

Missing: Dave Armstrong, Kent Ng, Kevin Gorman, Tapan J Chakroborty, Tom Waayers, Saman Adham, Bill Huott

Agenda:

- 1) 11:00 Brief update on Listserv from IEEE
- 2) 11:10 Open discussion on concepts/slides
- 3) 11:45 New Business
 - a. Poster Session at ITC
 - b. Meetings for next two weeks, cancel? Friday?

Meeting Called to order at 11:05 am EST

Minutes:

Update on IEEE Listserve

CJ sent out a test message today.

IEEE said that it should be up and running by 6pm today. CJ wasn't sure of the time zone though.

CJ Opened up the meeting to the rest of the group to get feedback on the information discussed at last week's meeting.

No one had any questions or comments at the moment.

CJ reviewed the slides that he sent out prior to the meeting to present to the new people in the call what the working group's scope and objective is.

CJ - Scope – to reuse a High Speed IO and use it for test data delivery. With the recent changes to 1149.1 we have the ability to configure the HSIO so that it could deliver data. Prior to the changes for 1149.1 you only had the compliance pins which wouldn't be sufficient to make this reuse happen.

CJ – Review of changes to 1149.1-2013

Ability to configure IO

Register segmentation and Power Domain control

Clamp Hold – lets you clamp and hold IO and load new instructions into the instruction register

CJ – In 1149.10 we want to deliver high speed test data. No standard existing yet. The idea is to reuse SERDES Phys that already exist in the devices today.

Standard will not be specifying the speed of SERDES

There will most likely need to have some test that occurs for the SERDES to make sure it works.

Need to have a generic method as all chips don't have the same SERDES

CJ – Interleaved packet format is probably going to be the best way to go

Slide 21 shows this packet.

Frans – How would you relate this to a network on a chip?

CJ – haven't given it much thought but would like to hear feedback.

Has only been thinking in terms of traditional scan based test

Frans –If you build small pieces of hardware, it comes down to ease of integration and overhead.

Frans – Sense you are showing the setup from 1149.1 standard. Does that mean we **need** 1149.1 before we can use this path?

CJ – currently yes. If someone had a SERDES that came up in 1149.10 mode and doesn't need to be configured than it wouldn't need it and wouldn't want to stop that from happening.

Marc – Would we give routing information in packet for data or would we use the TAP to define the route of the data.

CJ – Decoder would decode packet and route data. And tester will build a packet for scan information to get it into the decoder.

Would use Wrapper Serial Port(WSP) fields to define data fields.

Marc – so that would be the scan boundary controller that routes the data to specific sections of the chip and apply data and capture result

CJ – yes would be handled by the Packet Decoding and Distribution network.

Will need instruments on the chip to control the timing on the chip. This would require a packet to setup clocks and pulses first.

Frans – how does the test circuitry relate in size to current 1149.1 test circuit.

CJ - Packet Decoder and Distribution - Similar size to the TAP maybe a little bigger.

Hoping to leverage the CRC32 that should be there from the mission mode for the HSIO. And also leverage the 8b/10b 64/66b decoding that already exists in the HSIO.

Teresa – this is a very interesting idea. Can we get the University involved to do some experiments?

CJ – Sure. We are open to anyone who wants to participate. Was going to get Craig Stephan to provide a Verilog example.

Dwayne –would be interesting to see a proto type.

In reference to the CRC checking. What would you do if you did get an error?

CJ – we would need to look into it. You could resend it but that might not work correctly. Would need to restart shift over. May need to roll back to previous packets.

Dwayne – unless you buffer the packet and validate it before you operate on it you would need some roll back mechanism.

CJ – we could allow memory to store packets but might add too much infrastructure to test. Would not put into the standard that says you shall not do it however.

New Business

Poster session on ITC.

CJ will put together a poster and send to the group to discuss

Meetings for the next two weeks?

Should we cancel the next two weeks due to Labor Day and ITC?

Fans – would like to postpone meetings to allow time to digest information and discuss locally.

Teresa – will be out these 2 Mondays and the following 2 Mondays. Would vote for postponing.

Ismed- postpone as well

CJ – will hold on the 2nd and the 9th and regroup on the 16th.

CJ – we will review the Poster on the reflector.

Frans makes a motion to postpone next 2 weeks and make next meeting the 16th of September

Roger seconds

No one opposed.

Motion passes.

Mike – Thinks we are going in a good direction conceptually.

CJ – concerned about how to do the on chip timing. Doesn't think the standard should define that. Leaving it as a block for now.

Mike – wants to understand better what the bandwidth benefits are. Doesn't feel that there is a benefit of the SERDES until you move a lot of data.

CJ – Thought there were a lot of scan chains in chips and many parallel chains.

Mike – shift frequencies are not changing on chips. Chains are they way on chip today because of TAP.

Overhead from SERDES and packet decoding. Doesn't feel there are benefits until you start moving large amounts of data.

CJ – efficiency in packet will be good. Bottle neck will be in scan chains.

Motion to adjourn - Roger

Seconded - Frans

Meeting adjourned: 12:07EST.

Action Items

Next Meeting:

September 16th, 2013 11:00am

IEEE 1149.10- 2013 HJTAG Working Group Minutes

NOTES:

1149.10 working group website - <http://grouper.ieee.org/groups/1149/10/>

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