Date – 9/23/2013
Attendees: CJ Clark, Adam Ley, Bill Tuthill, Brian Turmelle, Craig Stephan, Dharma Konda, Frans de Jong, Gobi, Gurgen Harutyunyan, Josh Ferry, Kevin Gorman, Ismed Hartanto Marc Hutner, Mike Ricchetti, Philippe Lebourg, Roger J. Sowada, Steve Sunter, Tapan J Chakroborty, Saman Adham,

Missing: Dave Armstrong, Kent Ng, Tom Waayers, Bill Huott, Teresa McLaurin, Dwayne Burek,

Agenda:

11:00 Website update. Our website is at http://grouper.ieee.org/groups/1149/10/
This is the initial look with minutes and presentations. It will be updated as we progress.
11:15 For today's discussion I am teeing up this block diagram of the on-chip distribution network.

Meeting Called to order at 11:08 am EST

Minutes:

Website Update

Website for group is up and running. http://grouper.ieee.org/groups/1149/10/

Contains

- Motions Spreadsheet
- Minutes
- Technical Proposals and Discussion

Will add a spot for Attendance

Discussion of Block Diagram of the on-chip Distribution network that CJ sent out via email

- Left Side shows the data from SERDES interface (40 bits for example)
- SI/SO from the TAP interface
- Instruction decode to tell distribution matrix what chain to talk on for 1149.1 (can be any width. 4 bits in diagram is only example)
- P1149.10_enable enables from SERDES to scan chain. Or when not enabled can use traditional interface
- Right hand side is test data registers or wrapper serial ports. No limit to the number of wrapper serial ports.

- Also has a parallel interface (n bit wide) on right side.
- CSU is Capture/Shift/Update
- Packet decode and distribution matrix needs rules to describe it without describing any wires or gates

Frans – Either or dot 1 from the top or high speed IO from the left side. Can you imagine the combination can also be in the block to high speed io that is translated to tap signal so the tap controller is still in between. So you have both options.

CJ – Going after the same objective of compatibility.

Frans – the tap can be inside the block. SPI or I2C internally they are translated into tap signals. So it is just an interface on top that changes.

Steve – an embedded tap that has to run at high speed

CJ – it's an idea. The tap is on the side providing to allow the tap to function as it normally does. We are going to speaking on the same TDRs that the tap would be speaking on. Initial reaction is that the packet decoder is very non tap based. Not synchronous to a clock.

Frans – You still need the DOT1 connectivity to control the initial settings. Will DOT10 get rid of the tap on the top and live only by the high speed interface?

CJ – remains to be seen. Initial concept is really for the larger SOC's that will have a tap and SERDES on them already as opposed to smaller devices that may be pin limited. The idea is to reuse the mission mode SERDES and you would need a method to put the SERDES into a mode that is compatible with this standard. A single compliance pin may be difficult to do for this. To get the SERDES into the test mode is the challenge.

Steve – hard to see how Frans implementation is dot1 compliant without tap pins.

CJ – maybe we don't need to be compliant to 1149.1 because there is no TAP.

Steve – would have to test SERDES before you can use the port. The TAP controller has proven to be very reliable. Starting with SERDES only (no TAP) would be challenging

CJ – could have wrapper around the packet decoder and distribution matrix to use for testing. Need something to test the fabric we are using.

Frans- have serial interfaces that translate to the tap. Can call a device like that JTAG compliant but it is internally. In Dot10, would it be an option that dot 1 be declared.

CJ – remains to be seen. What the working group wants and what is reasonable as to whether the tap is there or not.

Steve – nothing from stopping the TAP from being an embedded tap.

CJ – initial momentum should be behind having an 1149.1 TAP to get completed in a reasonable time. However if it changes along the way we can explore that.

Steve- clocking that would go out to the wrappers. For example if it wasDOT1 you would have clock DR and update clock. Does the CSU include the clock or 2 clocks like regular dot 1.

CJ – 1149.1 is test clock and capture shift updates states.

Steve –There are no test clock shown in the block diagram. Clocking is the trickiest

CJ – The clock that is from the high speed interface is being derived and not from tap. In high speed data you would have a clock from the packet decoder for itself and from there you will have synthesized your clocks for your wrapper serial port.

Steve – right. Each port on the right will have a clock either a TCK or recovered clock from SERDES

CJ – not sure we have to use the recovered clock from SERDEs

Steve – Believes you do. For the proper timing you need to use the SERDES recovered clock. If it is not the identical frequency than data is accumulating somewhere.

CJ – do we need to specify that?

Steve – The point is going to be that there will be a high rate clock and it will be derived from the SERDES (or identical frequency)

Marc – just need to state in standard that the clocks need to be correlated. Agrees with Steve

CJ – We could state that you use the recovered clock.

Steve- we should save the clocking discussion. Just wasn't shown on the diagram and wanted to bring attention to it.

Steve – why use the 1149.1 tap controller and not hard code setup information.

CJ – so you can also send scan data to the chain. Use the tap to setup up INIT DATA register.

Steve – So all the registers that one can write through with a tap can also be accessible with the high speed interface.

Steve – what about the instruction register? If you can't control that through the HSIO will that be a problem. The instruction register will point to the register you want to write to.

CJ –You can write to the Instruction Register through the packets and packet distribution system.

Steve – the dot10_enable comes from a TDR

CJ – would be a bit that is in the INIT DATA register. It is the selector between mission mode and dot 10 mode.

Steve – you have an output that drives the INIT DATA so INIT DATA can be coming from Packet Data or from the TAP controller.

CJ – to get the SERDES into dot10 mode. So we are setting a bit for enable and configure the SERDES. So the INIT DATA is critical to get the SERDES into test mode

Saman – cannot load GotoMeeting on pc and may not be able to contribute to the meetings

Steve – might be able to open a WebEX to share GotoMeeting.

Saman – There is an underlying assumption that the SERDES works to use it for testing.

CJ – It's like any other test mechanism. Just like the TAP, you need it working in order to use it.

Saman – TAP is not complex timing wise to make work.

CJ – would like to use TAP to test circuitry.

Saman – trying to make it clear that the SERDES works. Standard isn't addressing the test of the SERDES and using the SERDES as the access mechanism to run the test. It wasn't clear in the PAR. That the underlying assumption that it works to make use of it.

CJ – in dot1 there isn't anything in there about the TAP needs to work before using it.

Ismed – timing of Scan In and Scan Out of this block – is it going to be specified where the edge will be on the right hand side.

CJ – that timing would be 1500 and 1149.1 based timing. It is a scan chain but follows 1500/1149.1. It would follow the timing referenced from those 2 standards.

CJ – want behavioral descriptions instead of implementation rules. Referencing the rules in 1500 or 11491 should be enough.

Tapan Motion's to adjurn

Seconded Ismed

Meeting adjourned: 12:01EST.

Action Items

Next Meeting:
September 30th, 2013 11:00am

NOTES:

1149.10 working group website - http://grouper.ieee.org/groups/1149/10/

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