

# High Speed JTAG IEEE 1149.10 High Speed JTAG Working Group Minutes

## **Date – 11/11/2013**

**Attendees:** CJ Clark, Adam Ley, Bob Gottlieb, Craig Stephan, Bill Tuthill, Brian Turmelle, Dharma Konda, Dwayne Burek, Frans de Jong, John Colburn, Josh Ferry, Kevin Gorman, Ismed Hartanto, Marc Hutner, Teresa McLaurin, Zahi Abuhanmdeh, Jim Wilson,

**Absent with Excuse:** Gurgen Harutyunyan, Mike Ricchetti,

**No Present for ¾ of meeting:** Dave\_Armstrong, Gobinathan Athimolom,

**Missing:** Kent Ng, Tom Waayers, Bill Huott, Tapan J Chakraborty, Saman Adham, Philippe Lebourg, Steve Sunter,

## **Agenda:**

- 1) Patent Slides
- 2) Is there a Motion to accept P&P Rev 4 sent to reflector?
- 3) Bandwidth discussion slides
- 4) Further discussions on packets
- 5) New Business

## **Meeting Called to order at 11:10 am EST**

### **Minutes:**

Review Patent Slide – Slide Presented to the Group.

Solicited input from anybody who is aware of patents that might read on our standard.

No Response

Quorum met. 13 out of 17 eligible members present

Online meeting program changed to live meeting.

### **Policies & Procedures Rev 4**

Adam makes a motion to accept latest changes of P&P sent out to reflector

Brian seconds.

Discussion: no discussion

Yes

Bill T	Dharma K	Kevin G	Adam L
Brian T	Dwayne B	Josh F	Bob G
Craig S	Ismed H	Teresa M	Zahi A

NO

Abstained

Frans

12 yes. 0 no. 1 abstain

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Bandwidth discussion slides.

CJ gave overview of slides sent to reflector.

Zahi – solution has to work at wafer probe. What is possible physically and economically? 11Gb/s is possible but expensive. What would this look like?

CJ – will be a challenge as speed goes up. One could go at the slower rate and multiply with channel bonding to get higher bandwidth.

Dave – 11Gb/s is harder and ATE aligns with PCIe.

No reference to 8Gb/s

Adam – Does channel bonding using multiple pins on a single UUT for bandwidth expansion?

CJ – yes.

Channel bonding might make sense to get the high bandwidth at the cost of more pins.

Distinct different between multisite test and channel bonding.

Zahi – How much does it cost to build a 2.5Gb/s SERDES probe vs. a 25Gb/s probe?

Would Guess there is a big difference in cost

CJ – does anyone have a feel for that?

Bob – 25Gb/s is difficult

Zhai – 5Gb/s is doable. Higher is more difficult.

25Gb/s SERDES's footprint on ASIC is huge amount of real-estate.

Might be good to have a 3<sup>rd</sup> dimension that shows the cost of silicon area

CJ – we are hijacking the SERDES that is already there for mission mode. Not suggesting adding an extra SERDES for only 1149.10

Dave – for today the standard at wafer probe is 5Gb/s and below

Call for new Business

No response.

Dwayne – good to have an update from ATE industry or Probe industry. Get some “state of the art” road map to see where ATE vendors are going.

CJ – will take an action item to reach out and get a presenter to give us an update

Dwayne – Broadcom has a history in protocol aware.

CJ – would like to hear what your thoughts are. Can you put something together?

Dwayne – will see.

CJ and Dwayne will talk offline to see if they can set something up.

Frans – feels we are making good progress.

And Moves to adjourn

Dave – seconds.

**Meeting adjourned: 12:00 EST**

*Motion Summary*

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Motion to accept latest changes of P&P sent out to reflector  
***12 Yes 0 No 1 Abstain***  
***Motion passes***

### ***Action Items***

***Bill Tuthill*** ~~10-21-2013~~ ~~Add minutes and Attendance spreadsheet to the website.~~  
***CJ*** 11-11-2013 *Reach out to ATE industry and Probe Industry to get update on future of ATE equipment to see which data speeds and protocols they are heading towards.*

### **Next Meeting:**

November 18<sup>th</sup>, 2013 11:00am

### **NOTES:**

1149.10 working group website - <http://grouper.ieee.org/groups/1149/10/>

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#### **Notes**

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