Date – 01/06/2014
Attendees: CJ Clark, Adam Ley, Bill Tuthill, Brian Turmelle, Craig Stephan, Dharma Konda, Dave Armstrong, Dwayne Burek, Gobinathan Athimolom, Frans de Jong, Jon Colburn, Josh Ferry, Mike Ricchetti, Steve Sunter, Tapan J Chakraborty,

Absent with Excuse: Bob Gottlieb, Gurgen Harutyunyan
Not Present for ¾ of meeting:

Missing: Kent Ng, Tom Waayers, Bill Huott, Saman Adham, Jim Wilson, Carol Pyron, Kevin Gorman, Ismed Hartanto, Marc Hutner, Philippe Lebourg, Zahi Abuhanmdeh, Teresa McLaurin,

Agenda:

1) Patent Slides
2) Update on Advantest response on Call for EP.
    a. Dave has sent me the signed LOA for 7,137,053
    b. 2 additional patents are included in LOA 7,412,639 and 7039545.
3) Affiliation record. Still need to get announced affiliation of several members
4) Removal of flow control packet in favor of flow control characters.
5) New Business

Meeting Called to order at 11:02 am EST

Minutes:
Review Patent Slide – Slide Presented to the Group.
Solicited input from anybody who is aware of patents that might read on our standard.
No Response

Advantest Response:
Dave Armstrong sent the signed LOA for patent 7,137,053 and also included patents 7,412,639 and 7039545 in the LOA

Affiliations
Dwayne Burke – Broadcom

Removal of the Flow Control Packet.
Flow control in our system will not work well due to the lack of storage for the serial packet.

Use of the K character will work for flow control.
Frans – Any reusable knowledge from the network community.

CJ – yes. SERDES, SRIO. Also SATA. SATA has an XON/XOFF frame.
These protocols however are used in systems with more resources that we have at our disposal.

CJ - If the receiver detects a CRC, than there is a failure. Will have to go back into the test. Back to the last reset/initialization sequence. Tester will have to know that.
The chip will have to detect that error based on CRC.
Dave had mentioned that you need to know the difference between a dropped bit and an actual error.
Would not be able to retransmit a whole packet though.

Dave – if we have a sequence that can't be reset and restarted , test don't always flow in a consistent fashion. Retesting for a dropped bit isn't a big deal. Would be doing infrequently. If we don't have the ability to retest for different reflow sequences we will have a problem.

CJ – not saying we won't have the ability to retest but not the ability to resend the frame.

Dave – the test is repeated. Data integrity with the SERDES approach should be good.
CJ – agreed.
CJ – if you are only looking at the CRC errors you won't be able to discern a bit drop from chip failure. You need to look at expected data as well to see if a bit was dropped or if there was a chip failure
Tapan- what do when you see a CRC error? Does it point to a problem in the interface of the chip?
CJ – A CRC is being calculated by the chip for the data that it is transmitted back. The CRC received by the tester has to match the data received by the tester.
Tapan – do you think there are any other mechanisms need to help debug the failure?
CJ – sure. Need to check SERDES first. Any other tests to check JTAG interface integrity after the SERDES is up and running.
Standard itself isn't going to dictate a SERDES BIST. Simply implanting a protocol in chip to transmit the scan data.

Steve – to say we can't interrupt the scan data in midstream, wouldn't make a different if we detect in CRC32. If there are any errors at all we can choose to rerun the test. If we get an error again we can say chip fails. Then we don't need to get involved in every protocol (encoding). If we get any errors we have to rerun failing segment of test and doesn't matter how we detect that error and can use a method outside the coding technique. If we get involved in all the encoding techniques, it would be a moving target. Would we have to keep incorporating the new techniques? We could divorce ourselves from the encodings.

CJ – The tester will still have to know about the encodings.
Steve – could say in the standard that the encoding is provided.
CJ – agreed.

CJ – we do need to define what to use for Xon/Xoff. How does the tester know what the special character is and what it's meaning is. Could use an extension in BSDL.

Steve – normal testing we are testing the SERDES and expect variations. But with the scan test we have a pretested SERDES and should meet specifications and not interested in testing the SERDES. Are we expecting errors?
CJ – no we are not expecting errors, but we are making contact to the wafer and at 5GB/s we could have transmission errors that occur due to noise or something else with the Wafer.
Steve – all those problems are not unique to SERDES.

Dave – a lot of the failures are determined by the SERDES itself and would retrigger a valid transmission. The probability of a SERDES error is very low. I think we are better off than we should be. We can do a CRC on the input data stream and the output data stream.

Steve – errors in the CRC are indicating an error in transmission. And we can choose what action we take. And not worry about encoding.
CJ – Can't just look at CRC. If you look at CRC only it will be different from what you expect and from a bit error. You need to look at each bit that you receive and calculate the CRC.
Steve – chip core is producing the scan data. The Core of the chip conveys that information to the SERDES transmitter and a CRC is created. And the tester looks at the payload data and the CRC. If the tester sees a CRC data it knows that there was a transmission error. If the CRC is good than it looks at the payload data to determine if there was a bit error. If the CRC is wrong than we know that it was a transmission error.

CJ – with flow control we would need a way to slow down the bits going in and out of the chip
Steve – we are doing test. We know the details of the test. We know the clock rate and scan chains. We would know how to run the test to not over the device.
CJ – Style has clock information in it. And we could predetermine how much data to send in for each operation. See some technical data there. Flow control is a method for the chip to communicate that you are sending too much data.
CJ – see the clock frequency changing for the chip and the SERDES clock being different. Sees the K character easier as it would be separated from the chip specifics.
CJ – if we implement Xon/Xoff we don't have to use it. You could preformat your data to the right size. But if you have it than it can be used by a tester capable of using it.
Dave – Agnostic – likes Steve's idea of being protocol agnostic. Don't think we can be "Chip Agnostic" Can't have a single scan interface servicing a single core at a time. We won't be able to get there.
CJ – the PAR is to develop a protocol and packet decoder. Why would I care from a standard perspective we don't care if we have 1 or many cores. Why is there a focus to only work with multiple cores?

Dave – As part of our protocol we should have the command of the structure to say that that data stream is able to feed multicores in parallel.
CJ – we are doing it but in a different way. We are doing low level packets of scan data. Where it goes in the chip is up to the DFT of the chip. We don't have packets based on tests but how to encapsulate the Scan Data.

New Business.
No New Business

Motion to Adjourn : Steve
Seconded : Dave

Meeting adjourned: 12:15 EST

Next Meeting:
January 13th, 2014 11:00am

Motion Summary

Action Items
~~***Bill Tuthill – 10-21-2013 -Add minutes and Attendance spreadsheet to the website.***~~
~~***CJ 11-11-2013 Reach out to ATE industry and Probe Industry to get update on future of ATE equipment to see which data speeds and protocols they are heading towards.***~~

NOTES:

1149.10 working group website - http://grouper.ieee.org/groups/1149/10/

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Notes

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