

IEEE 1149.10 High Speed JTAG Working Group Minutes

Date – 03/03/2014

Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Craig Stephan, Dharma Konda, Dwayne Burek, Frans de Jong, Gobinathan Athimolom, Ismed Hartanto, Jon Colburn, Josh Ferry, Marc Hutner, Roger Sowada, Steve Sunter,

Absent with Excuse : Dave Armstrong, Tapan J Chakraborty,
Not Present for $\frac{3}{4}$ of meeting:

Missing: Bill Huott, Carol Pyron, Jim Wilson, Kent Ng, Kevin Gorman, Saman Adham, Tom Waayers, Heiko Ehrenburg, Gurgen Harutyunyan, Zahi Abuhanmdeh, Philippe Lebourg, Bob Gottlieb, Adam Ley, Mike Ricchetti, Teresa McLaurin,

Agenda:

- 1) Patent Slide
- 2) Discussion of Clause 4
 - a. Discussions of compliance enable pins.
 - b. Similar to 1149.1 compliance pins but we have already two compliance enablement methods. Do pins strapped at the board level to enable SERDES mission mode, now prevent use of 1149.10 at board/system?
 - i. This would go contrary to the objective of having re-use
- 3) New Business

Meeting Called to order at 11:05 am EST

Minutes:

Review Patent Slide – Slide Presented to the Group.

Solicited input from anybody who is aware of patents that might read on our standard.

No Response

Draft 5 was put in the private area on the IEEE 1149.10 website

Clause 4

High Speed Access port

3 Methods to get into compliance mode.

- 1) 1149.1 interface to enable 1149.10 mode
- 2) Compliance enable pins
- 3) Powers up in 1149.10 state

Marc - Would you be able to figure out from the BSDL how to initialize the chip?

CJ – yes the BSDL would have attribute compliance of dot 10

Adds come confusion towards pins strapped at the board level and can't use them.

Section 7.5 Compliance Enable.. Lifted from 1149.1 compliance attribute

Frans – rule C – if user is expected to power up chip and sends config packet you would be in test mode?

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CJ – would have to form a specific packet. Yes. You would be in test mode.

Another method of enabling would be to send a character over USB or PCI Express not used in mission mode could enable port and allow you to send in config packet.

Steve – 1149.10 offers a way to get to the core of the chip in test mode.

CJ – not different than 1149.1 TAP. Can get access to core with 1149.1

Steve – do we allow dot 1 tap not to exist? If you don't have the 1149.1 TAP than you could cut off access to the 1149.10 TAP. Wants to prevent a hack over the WEB because of SERDES interface (software port) .

CJ – would like to give flexibility for people to build the way they want. 10 years down the line, no one may want a slow TAP interface. Will want a high speed interface only.

Could encrypt what I'm sending. Not sure we need to address all the options.

Frans – maybe we could put in note at the clause where the dot 1 TAP could be used for security.

CJ – a 1149.1 TAP would be a weak security interface. Maybe as securing remote access. But not much security at the board level.

Steve – A 1149.1 interface has a hardware lock. You needs physical access.

Frans – if people need this they can have a 1149.1 interface.

CJ – A rule saying to use it may not be fair.

Steve- Not comfortable creating a chip that has no 1149.1 TAP at this stage.

CJ – OK. The TAP isn't the only interface that can communicate to things. Might not have enough pins to have a separate TAP.

Steve- compliance pins would help with the Security concerns.

CJ – it's all good feedback. There will be a time where TAPs are not sufficient. They are too slow.

Steve – don't buy the slow argument. You would have a 1149.1 AND a 1149.10 TAP.

CJ – both are allowed but you are not required to have 1149.1 tap. For FPGA configuration is too slow today over a 1149.1 interface.

Steve – use 1149.1 tap to turn on 1149.10 TAP and use the 1149.10 TAP to program the FPGA.

CJ – you are required to put down 4 more pins.

Steve – 4 more pins is trivial on an FPGA.

Steve – 1149.10 should keep a 1149.1 TAP as part of the standard

CJ – would like to have the standard move beyond a 1149.1 TAP and not have that required for operation

Josh – How would chaining look in high speed taps?

CJ – chaining of 1149.10 interfaces has been designed. Purpose of the targeting packet.

Frans – Functional point of view. Steve's points are about safety (security) and do you need a TAP if 1149 is in the name of the standard. Not sure. 1149 name gives certain expectations but not sure that is needed.

CJ – doesn't feel that is a rule that the 1149 name requires a 1149.1 TAP.

If you want to put in an 1149.1 TAP that you are allowed to do so.

If you want to just have the HighSpeed interface for 1149.10 than that is allowed as well.

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Steve – testing a board with mixed devices would be difficult. 1149.1 chips would be daisy chained. 1149.10 devices would be sitting on their own. Would be multiple interfaces that would have to be tested. Not one simple chain.

CJ – 1149.10 would allow more testing as it would allow another interface for vendors to have access to cores for devices that don't have a TAP.

Steve – 1149.10 doesn't bring anything for chips that just have functional test and no TAP.

CJ – if there is a 1149.10 interface it would give you access to the core/registers of the chip.

Steve- chips that don't have the 1149.1 interface are not candidates for 1149.10.

Frans – had some ASICS that would take too long with Scan Test 1149.1 could do with high speed tests now

Learn from the past and invent new things for the future.

Is it usable and that is a difficult discussion and needs some careful discussion.

CJ – does anyone want to make a motion about a SHALL have a TAP or converse that SHALL NOT have TAP

Frans – still unclear for a motion. Still open to the option to have it or not.

CJ – don't think that TAPs will be immediately dropped but might allow those devices without a TAP to have a standard way to communicate with the core.

Frans – should we have a discussion with our IEEE sponsor on this?

CJ – I welcome anyone to have that conversation but don't feel it is necessary.

Steve – scope of 1149.10 says it includes 1149.1 BSDL. Can you do a BSDL without a TAP

CJ – yes we can.

Steve – scope implies we will have a 1149.1 TAP

CJ – not reading it that way. Clause 4/5 comes from the 1149.1 standard. Not from the BSDL language.

Steve – how do you write BSDL for something that doesn't have a TAP?

Dwayne – some elements in the BSDL require a 1149.1 TAP

CJ – rule 7.1.1.a says that we are not required to have a scan port identification.

Dwayne- can't call it 1149.1 BSDL then?

CJ – Standards that build off a language can add or subtract.

Steve- if you can strike whatever you want and add whatever you want it wouldn't be a BSDL anymore?

CJ – don't see the need to replicate all of BSDL because we are not using 1 piece. Want to use pieces that are already well defined. Since 1149.10 doesn't require the 1149.1 TAP we removed the 1 section that requires a 1149.1 TAP and allows us to reuse BSDL.

Dwayne – would the dot 10 interface have a specific compliance pin? To drive it in automatically, that would be allowed? I think that would cover it for me if you didn't have a 1149.1 interface.

CJ – would prefer the method of sending the character into the interface to enable the 1149.10 interface. Concerned the pins would be strapped incorrectly at the board level.

Dwayne – class of components that don't want 1149.1 interface (don't want pins). Don't see it as a value to carry.

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CJ – right. From my experience I see a lot of components that don't want a TAP.

Motion to Adjourn: Brian
Seconded: Frans

Meeting adjourned: 12:00 EST

Next Meeting:
March 10th, 2014 11:00am

Motion Summary
0 motions made

Action Items

~~Bill Tuthill – 10-21-2013 – Add minutes and Attendance spreadsheet to the website.~~
~~CJ – 11-11-2013 – Reach out to ATE industry and Probe Industry to get update on future of ATE equipment to see which data speeds and protocols they are heading towards.~~
Philippe – Look into alternative method to create control information (pause, start, terminate, etc.) rather than using K characters in packet.
Bob – create a case study to show use of Attributes
Frans – will start some block diagrams of a simple use case to help illustrate the current architecture
Dwayne – present to the group his ideas for a simplified scheme – Direct Interface.

NOTES:

1149.10 working group website - <http://grouper.ieee.org/groups/1149/10/>

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