Date – 08/11/2014
Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Craig Stephan, Dharma Konda, Frans de Jong, Gobinathan Athimolom, Ismed Hartanto, Jon Colburn, Josh Ferry, Marc Hutner,
Philippe Lebourg,

Absent with Excuse : Bob Gottlieb, Tapan J Chakraborty,
Not Present for ¾ of meeting:

Missing: Bill Huott, Carol Pyron, Jim Wilson, Kent Ng, Kevin Gorman, Tom Wayers, Heiko Ehrenburg, Dave Armstrong, Roger Sowada, Dwayne Burek, Zahi Abuhanmdeh, Mike Ricchetti, Saman Adham, Gurgen Harutyunyan,
Adam Ley,Teresa McLaurin, Steve Sunter,

Agenda:

1) Patent Slide
2) Discuss moving to 64 bits for RAW packet or using "0" to mean "infinite". Original RAW packet had no limit, it was asked for a value such that at the end of packet data, SERDES channel went back to P1149.10 packet mode.
    a. Motion for 64-bit <count>?
3) Latency: how best to define? This is the amount of delay the TX has compared to the RX not including the data rate time to transmit. After RX word is received how much time before TX starts to transmit associated response?
4) New Business
5) Adjourn

Meeting Called to order at 11:00 am EDT

Minutes:
Review Patent Slide – Slide Presented to the Group.
Solicited input from anybody who is aware of patents that might read on our standard.
No Response

<u>Review of 6.5.1 Count value</u>
Count is the number of bytes to send over PHY
Currently sized for 32 bit
Do we want to expand to 64 bits?
Cons
Counter would have to be optimized do 64 bits. Could be difficult for some architectures
If you put 64 bits, could have a long time frame. Be forced to use reset to get out of mode
Alternative would be to assign zero value to mean "no limit"

Would allow for long BER test.
Marc – Zero being endless doesn't sound good
CJ – with 64 you would be effectively endless
For characterization of ATE set up is it bad to cycle power to get out of this mode
Marc – cycling power is bad. You do want to get out of the mode though.
Marc – with BER, it doesn't make sense for ATE to generate data for BER because it's Algorithmic.
CJ – agreed for a production test it isn't practical. This is more for a lab setup. To verify signal integrity.
Marc – would till push that it is Algorithmic. Wouldn't envision it being a signal packet that has a huge count associated with it.
Jon – assume that setting this to infinite and the cost of doing power on reset is fine. The overhead for 4 hour testing doesn't seem like it would matter.
Jon – could a Dot 1 TRST bring us out
CJ – Not at this time it doesn't. Can provide a mechanism to have an 1149.1 disablement capability. Maybe not TRST. Might want to enter the TRST and not disable it. Might want to scan and monitor a register while the BER is running.
Jon – would be fine using the TAP and not just using TRST.
Frans – 32 bit would be enough if it can be repeated as many times as you want.
CJ –action can be nothing if that is what the group settles on.
Marc – as long as there is a way to describe how the ATE can exit the infinite mode.
CJ – Could write up some PDL to show as an example if this is what the group is leaning towards.
CJ – hearing from the group that 32 bits is fine and have a Infinite mode defined with a value of "0" in the count field. And have a Tap method to bring the device out of the Infinite mode and stop the test .

<u>Latency</u>
In HSTAP the latency is described as maximum delay associated with the response of the TX to received data at the RX.
Trying to describe the delay from the Receiver receiving the data from the Transmitter.
Bob and Steve had comments that it wasn't clear what Latency is. (Referring to description)
Marc – have the control packet coming into the chip on the receiver. What is the latency on that control packet coming back at you? This is a no memory protocol (standard). As soon as you scan in something you should be able to scan out data. Latency is the assertion of the control packet coming back at the tester when knowing that you are inserting something in the tester at a certain cycle.
CJ – Right. It is a certain amount of time that data comes back from the chip to the tester after the transmitted data being received at the chip.
Marc – sending back control header saying here is my real data. Gross latency and a variation associated with it that is why you would have the header data coming back.
CJ – each packet we send in has an associated return packet with it with an SOP. So you would know when your data is coming back.

Frans – latency is something you provoke through the test. There is a max and minimum value specified. Is that defined here.
CJ – might make it unpredictable?
Marc – the Max is the length of your IDLE packet coming back at you.
Its plus some time that you know you will get a response.
Think we can come up with an equation given some of the logic in the chip.
CJ – there is a window (based on Frans' suggestion) and you should be able to define in the tester that window and there would be a formula based on the data rate.
Marc- we know when the end of the request packet and the beginning of the request back plus the clock coming into the device. If we know the max and min we could create a window around it that would make sense.
Marc – window would be important to know when to stop looking for data and fail the test.
CJ – in BSDL will update the grammar to have a min/max on LATENCY

Call for New Business
No new business

Please use reflector to review what is in the Draft.
Please send comments to reflector.
Anything that needs to be updated or you would like discussed

Motion to Adjourn: Marc
Seconded: Frans
Meeting adjourned: 11:49 am EDT

Next Meeting:
August 18th, 2014 11:00am

Motion Summary

0 motions made

Action Items
~~Bill Tuthill – 10-21-2013 -Add minutes and Attendance spreadsheet to the website.~~
CJ 11-11-2013 Reach out to ATE industry and Probe Industry to get update on future of ATE equipment to see which data speeds and protocols they are heading towards.
Philippe – Look into alternative method to create control information (pause, start, terminate, etc.) rather than using K characters in packet.
Bob – create a case study to show use of Attributes
Frans – will start some block diagrams of a simple use case to help illustrate the current architecture
~~Dwayne – present to the group his ideas for a simplified scheme – Direct Interface~~.

NOTES:

1149.10 working group website - http://grouper.ieee.org/groups/1149/10/

Here is the WebEx conference link.

https://meetings.webex.com/collabs/meetings/join?uuid=MAG12PB7HN5W24AM2EOKIOM9KS-KERT

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