**Date – 12/08/2014**
**Attendees:** CJ Clark, Adam Ley, Bill Tuthill, Bob Gottlieb, Brian Turmelle, Craig Stephan, Dharma Konda, Gurgen Harutyunyan, Jon Colburn, Steve Sunter, Tapan J Chakraborty,

**Absent with Excuse**: Frans de Jong
**Not Present for ¾ of meeting**:

**Missing:** Bill Huott, Carol Pyron, Jim Wilson, Kent Ng, Kevin Gorman, Tom Wayers, Heiko Ehrenburg, Dave Armstrong, Roger Sowada, Dwayne Burek, Zahi Abuhanmdeh, Mike Ricchetti, Saman Adham,
Teresa McLaurin, Philippe Lebourg,
Josh Ferry, Gobinathan Athimolom, Ismed Hartanto,
, Marc Hutner,

**Agenda**:

1) Patent Slide
2) Motion to accept Clause 8 in draft 47
3) Discussion of Clause 5 changes.
4) Adjourn

**Meeting Called to order at 11:010 am EST**

**Minutes**:
Review Patent Slide – Slide Presented to the Group.
Solicited input from anybody who is aware of patents that might read on our standard.
No other responses noted.

Brian makes motion to accept clause 8 in draft 47
Bob seconds motion

Discussion
Tapan – Is the align character is subject to error condition as well. How do we detect error on align character.
CJ – no CRC on control character
Tapan – how do we detect this?
CJ – you wouldn't get the response that the lanes are ready for channel bonding
CJ – if we don't get the align character on a lane than we wouldn't continue. We would recognize the error. You don't get the align character back if we sent in corrupt data. You wouldn't see on the receiver the first align character coming back.
The rules say you need to respond with the align character
Bob – no capabilities to put in for a degraded performance. It's all or nothing based on how it is specified.

CJ – correct. The ATE could try again or fail.
Bob – no expectation to go in a half mode.
CJ – if someone wanted to do that, there are no rules in the standard to prevent that if they came up with a scheme.
Tapan – the higher level software will check for these and make a decision on what to do.
CJ – correct. The most likely scenario will be for the ATE will try again.
CJ – we don't specify anything regarding what should be done.
Tapan – beyond the scope of the standard
CJ – basic architectural rules. We send in something and get something back. But don't want to make anything restrictive.. Won't add rules in to prevent people from doing anything as long as it won't break anything.
Tapan – Writing could use a little more meat such as what we just discussed.
CJ – rules in b and c) are clear. Need to recognize that these have a response.
CJ – error character is required to come back if the align character is not to be sent back.
Bob – how often we need to be sending the align character? To take care of drift, where the skew would change over time?
CJ – in the BSDL you would specify the align character in the HSTAP BSDL attribute. You would document the min and max byte count. No way to say you need to send in x number of characters.
The ATE should always know how often to send the align character, but we don't say what that number is
Bob – so where in the standard do we specify the BSDL attribute? We specify the max byte count before we do another align character.
CJ – rule p) and q) section 7.2.2 rules
CJ – rule that requires the user to document this in the BSDL.

Call the question.
<u>Yes</u>

| | |
|---|---|
| Bill T | Dharama K |
| Brian T | Jon C |
| Craig S | Tapan C |

<u>No</u>

<u>Abstain</u>
Adam L
Steve S
Motion passes
7 – 0 – 2

Clause 5
Updated rule d) to add clarity.
Added roman numerals for subsections of the rule for consistency to DOT1
Bob – while in 1149.10 mode I can still access IR register. Up to the user to make sure nothing is clobbered between the two modes with the registers.
Why is there a restriction that when the 1149.1 TAP is in TLR it shouldn't be interrupted?
Once you enable DOT10 can't I be in any TAP state in 1149.1.
CJ – you can. This is minimum rule that being in TLR or RTL cannot interfere with the PEDDA. If you want to go beyond that is up to the user.
CJ – you are accessing through the TAP. If you have an IR that sets mode, not going to write another method to go through DOT10 interface. If you load different instructions in the Instruction Register you could have collisions.
Bob – would have some shared TDRs, but some unique TDRs on the 1149.1 side. If they are shared they will collide and up to the test writer and implementer to avoid collisions. For the unique ones its fine to have them going at the same time.
Bob – not saying that that in DOT10 mode we are going to block off the DOT1 access. Up to the programmer to manager the two.
Do we have to leave the mode of DOT10 to access shared TDR through DOT1?
What mode is the DOT10 in if we want DOT1 to access the TDR?

CJ – Any of the above. Minimum requirement that the TAP isn't interfering in RTL or TLR. Why would we access something through the DOT1 interface if we have the DOT10 interface? It is the faster interface.
Steve – Legacy PDL that goes through the DOT1 TAP and want to mix with the DOT10
You want to do some function through the DOT10 interface and you want to change the interface and the PDL was written to go through the DOT1 TAP.
CJ – on the fringe of the use model. Nothing in the PDL that is specific to the TAP. Would provide DOT10 access to those registers. And blast those commands through the DOT10 interface.
Steve – if you had legacy software that didn't understand the DOT10 interface.
CJ – no rule from doing it. It's coordination from a test engineer that would need to manage it.
Steve – is there precedence between the DOT1 and the DOT10 interfaces?
Bob – can't think of a case that we would be doing this is for registers that we keep separate. Think we would want to concurrently access different chains. Can't think of a case that we would want to switch back and forth between the two.
CJ – no priority. It would be whoever last accessed the registers.
Bob – if we designed this if we had shared chains we would have mux control and block the registers from DOT1
Steve- so it would be non-deterministic for who had priority.
Bob – would be up to the implementer.
CJ – to get to the TDR you need to get to load the instruction register.
Steve – designer of the chip will have to make one of the precedence.
CJ – if you have a register there is nothing that says there must be precedence

It's whatever value that is inside the register. And that is what will set the mux to what TDR you are looking at.
Bob – basically saying that shared resources and whoever programmed the IR is controlling the register.
Steve – you have a mux that is controlling that IR and the mux has to switch between interfaces. What happens if both are trying to control the mux?
CJ - you could write it without a mux.
If you want to run both at the same time than you will provide that OR situation.

Send any New Business requests to the reflector

Please use reflector to review what is in the latest version of the draft. Please send any comments on the new material to the reflector. This will let us get a start on the material before the meeting. Please include anything that needs to be updated or anything you would like discussed

**Motion to Adjourn: Steve**
**Seconded: Brian**
**Meeting adjourned: 12:03pm EST**

**Next Meeting**:
Dec 15th, 2014 11:00am

***Motion Summary***
***1 motions made***
Motion to accept clause 8 in draft 47
Motion Passes
7-0-2

***Action Items***
~~***Bill Tuthill – 10-21-2013 -Add minutes and Attendance spreadsheet to the website.***~~
~~***CJ 11-11-2013 Reach out to ATE industry and Probe Industry to get update on future of ATE equipment to see which data speeds and protocols they are heading towards.***~~
***Philippe – Look into alternative method to create control information (pause, start, terminate, etc.) rather than using K characters in packet.***
***Bob – create a case study to show use of Attributes***
***Frans – will start some block diagrams of a simple use case to help illustrate the current architecture***
~~***Dwayne – present to the group his ideas for a simplified scheme – Direct Interface.***~~
~~***Adam – invite someone from IEEE to speak on IEEE benefits of standardization at WG meeting***~~

Patent notes
Adam Ley 12/1/2014
PN, TTL, AN

7348796, METHOD AND SYSTEM FOR NETWORK-ON-CHIP AND OTHER INTEGRATED CIRCUIT ARCHITECTURES, DAFCA INC.

Steve Sunter 11/17/2014

1. US 7610532 “Serializer/de-serializer bus controller interface” Avago, granted 2009
2. US 7739567 “Utilizing serializer-deserializer transmit and receive pads for parallel scan test data” Avago, granted 2010
3. US 8543876 “Method and apparatus for serial scan test data delivery” Altera, granted 2014

NOTES:

1149.10 working group website - http://grouper.ieee.org/groups/1149/10/

Here is the WebEx conference link.

https://meetings.webex.com/collabs/meetings/join?uuid=MAG12PB7HN5W24AM2EOKIOM9KS-KERT

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