Date – 3/02/2015
Attendees: CJ Clark, Bill Tuthill, Bob Gottlieb, Brian Turmelle, Dharma Konda, Frans de Jong, Gobinathan Athimolom, Jon Colburn, Josh Ferry, Marc Hutner, Mike Ricchetti, Steve Sunter, Tapan J Chakraborty,

Absent with Excuse: Craig Stephan,

Not present for ¾ of meeting: Ismed Hartanto,

Missing: Bill Huott, Carol Pyron, Jim Wilson, Kent Ng, Kevin Gorman, Tom Wayers, Heiko Ehrenburg, Dave Armstrong, Roger Sowada, Zahi Abuhanmdeh, Saman Adham, Teresa McLaurin, Philippe Lebourg, Gurgen Harutyunyan, Adam Ley, Dwayne Burek,

Agenda:

1) Patent Slide
2) Stephen Sunter presentation on alignment
3) New Business
4) Adjourn

Meeting Called to order at 11:01 am EST

Minutes:
Review Patent Slide – Slides Presented to the Group.
Solicited input from anybody who is aware of patents that might read on our standard.
No other responses noted.

Steve Sunter's Presentation
Presentation emailed to reflector on 2/25/2015

Comma Character is a special character.. some question as to whether it was for alignment or clock recovery
PEDDA must do job for alignment
2 byte parallel port
Straight forward to align all fields to 2 byte parallel port.
PEDDA would know where each field comes in that 2 byte port.
Align fields to 16 bit boundaries.
SOP followed by IDLE or 2 SOPs
Would need to use IDLE pairs for alignment
Test delivering all these bytes. Tester will be synchronous to system clock. Could be free running. Control over how many IDLEs are inserted

4 byte parallel port
Count aligned to 32 bit boundary makes it easier.
8 byte parallel port

Padding. Should it be all zeros or any data
Forcing byte space after command would ensure that the TARGET ID could have all zeros for first byte.
For IDLE and SOP must fill up all 8 bytes

Proposed rules.
Objective – ensure it is possible to operate at SerDes parallel clock rate or slower, use DFT logic that is less complex than mission logic, and scan test all logic not in PHY
Rules shouldn't have any significant impact on through put
Must forward all control characters (including IDLEs)
Rate matching with system clock may propose a special problem.
Cannot mix 8b/10b, 64b/66b/128b/130b in single chain

Raw going by one end point can understand it. Sequence could be valid for something else in the chain though.
Bob - Raw only has one target we are talking to?
Steve – other non-target device is not expecting data coming down the line
CJ – raw was to allow you to do PRBS only applicable when you have the chip standalone.
Steve – could do pseudo random data bytes
CJ – could have different type of raw packet that does encoding and just send data in the packet format. But not how we have RAW currently defined
Bob – thinking we were using RAW to test where problem is when content isn't working.
CJ – the one that is defined is more to have chip on ATE by itself and want to validate signal integrity.
Steve – need to have PRBS data that is 8b10b encoded.
Bob – no one should be listening if not target.
Jon – can't come out of RAW until you finish data?
Steve – no mention if it is any data or data with control characters.
CJ – was intended to be purely raw and not predictable.
Bob – no EOP that comes with RAW packet?
Steve – yes.
CJ – packet is as how Steve shows it.
Steve – is invalid to send anything bigger than PRBS7 on 8b/10b
CJ – maybe we should have raw mode (and needs better definitions)

CJ – what is in draft 53 has most of this. Some minor differences in format.
Can we daisy chain with different alignment sizes?

Steve – should be able to cover different alignment sizes with same encoding

Motion to Adjourn: Steve
Seconded: Jon
Meeting adjourned: 12:00pm EST

Next Meeting:
March 9th, 2015 11:00am

Motion Summary
0 motions made

Action Items
~~***Bill Tuthill – 10-21-2013 -Add minutes and Attendance spreadsheet to the website.***~~
~~***CJ 11-11-2013 Reach out to ATE industry and Probe Industry to get update on future of ATE equipment to see which data speeds and protocols they are heading towards.***~~
~~***Philippe – Look into alternative method to create control information (pause, start, terminate, etc.) rather than using K characters in packet.***~~
~~***Bob – create a case study to show use of Attributes***~~
~~***Frans – will start some block diagrams of a simple use case to help illustrate the current architecture***~~
~~***Dwayne – present to the group his ideas for a simplified scheme – Direct Interface.***~~
~~***Adam – invite someone from IEEE to speak on IEEE benefits of standardization at WG meeting***~~

Call for Essential Patent notes
Adam Ley 12/1/2014

PN, TTL, AN
7348796, METHOD AND SYSTEM FOR NETWORK-ON-CHIP AND OTHER INTEGRATED CIRCUIT ARCHITECTURES, DAFCA INC.

Steve Sunter 11/17/2014

1. US 7610532 “Serializer/de-serializer bus controller interface” Avago, granted 2009
2. US 7739567 “Utilizing serializer-deserializer transmit and receive pads for parallel scan test data” Avago, granted 2010
3. US 8543876 “Method and apparatus for serial scan test data delivery” Altera, granted 2014

NOTES:

1149.10 working group website - http://grouper.ieee.org/groups/1149/10/

Here is the WebEx conference link.

https://meetings.webex.com/collabs/meetings/join?uuid=MAG12PB7HN5W24AM2EOKIOM9KS-KERT

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