

Date – 3/09/2015

Attendees: CJ Clark, Adam Ley, Bill Tuthill, Bob Gottlieb, Brian Turmelle, Craig Stephan, Dharma Konda, Dwayne Burek, Gobinathan Athimolom, Ismed Hartanto, John Braden, Jon Colburn, Josh Ferry, Marc Hutner, Mike Ricchetti, Steve Sunter, Tapan J Chakraborty,

Absent with Excuse: Frans de Jong,

Not present for ¾ of meeting:

Missing: Bill Huott, Carol Pyron, Jim Wilson, Kent Ng, Kevin Gorman, Tom Wayers, Heiko Ehrenburg, Dave Armstrong, Roger Sowada, Zahi Abuhanmdeh, Saman Adham, Teresa McLaurin, Philippe Lebourg, Gurgen Harutyunyan,

Agenda:

- 1) Patent Slide
- 2) Continue discussion on alignment
 - a. As Editor, I'm not sure how to proceed, yet
 - i. There have been some good refinements but I have some concerns about daisy-chain of HSTAPs
 - b. Craig and I have some material to present
- 3) New Business
- 4) Adjourn

Discussion on Alignment.

Review of slides presented by CJ

Possible need to add a "gasket" to help align data based on SOP

Craig has made a test case and compiled into Virtex 6 , Cyclone 5 and Lattice ECP and there is very little logic being used for this.. 1% or less (based on chip size)

Steve would like to minimize the logic AFTER the gasket. The PEDDA logic that distributes the data to the scan chains

Gasket needs to recognize where the data is coming in. If we standardize on 32 bit it would be easier for other multiples (64 and 128)

Steve would like to explore the implication downstream of the gasket. What is special about 32? Feels it's the backend of the PEDDA that the complexity is. Would like to see an example after the PEDDA to see the data path. Need the fields are coming out in a predictable way. Not sure where things will sit on different sizes. (64 or 128 if aligned on 32)

CJ – once it is aligned by the gasket for 32 bits it is predictable on multiple of 32 bits.

Steve – by standardizing on 32 you would need another gasket to sort it out for whatever the data size is after the gasket.

CJ – feels it is predictable after the gasket.

Tapan – a full example might clarify any issues that might be in the details

CJ – having a predictable format makes the validation engineer's job easier.

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CJ – would need to have logic to decode the packet. And decode the formatting of the data for the scan chain.

Tapan – those are the details

CJ – logic is no different if we format on 32 bits or variable alignment. It's not a gating factor.

Bob - 32 seems arbitrary.

CJ – can be anything

Bob – thought we would align the data to the biggest in the chain

CJ – no way to take the largest device in the scan chain and format for the largest alignment size.

Steve – this is why the SOP needed to be in the LSB

Dwayne – looks like are focusing on the input decode. We use a lot of compression, more issues on how to get the scan data out. Not sure if the cascading or daisy chaining is feasible. Need to encode it on the other end (scan response).

Bob – one of limitations is that we can't target 2 devices at the same time.

Dwayne – need to understand the output alignment and how to rebuild the packets.

Meeting Called to order at 11:00 am EST

Minutes:

Review Patent Slide – Slides Presented to the Group.

Solicited input from anybody who is aware of patents that might read on our standard.

No other responses noted.

Motion to Adjourn: Dwayne

Seconded: Craig

Meeting adjourned: 12:00pm EST

Next Meeting:

March 16th, 2015 11:00am

Motion Summary

0 motions made

Action Items

Bill Tuthill – 10-21-2013 – Add minutes and Attendance spreadsheet to the website.

CJ – 11-11-2013 – Reach out to ATE industry and Probe Industry to get update on future of ATE equipment to see which data speeds and protocols they are heading towards.

Philippe – Look into alternative method to create control information (pause, start, terminate, etc.) rather than using K characters in packet.

Bob – create a case study to show use of Attributes

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Frans—will start some block diagrams of a simple use case to help illustrate the current architecture

Dwayne—present to the group his ideas for a simplified scheme—Direct Interface.

Adam—invite someone from IEEE to speak on IEEE benefits of standardization at WG meeting

Call for Essential Patent notes

Adam Ley 12/1/2014

PN, TTL, AN

7348796, METHOD AND SYSTEM FOR NETWORK-ON-CHIP AND OTHER INTEGRATED CIRCUIT ARCHITECTURES, DAFCA INC.

Steve Sunter 11/17/2014

1. US 7610532 "Serializer/de-serializer bus controller interface" Avago, granted 2009
2. US 7739567 "Utilizing serializer-deserializer transmit and receive pads for parallel scan test data" Avago, granted 2010
3. US 8543876 "Method and apparatus for serial scan test data delivery" Altera, granted 2014

NOTES:

1149.10 working group website - <http://grouper.ieee.org/groups/1149/10/>

Here is the WebEx conference link.

<https://meetings.webex.com/collabs/meetings/join?uuid=MAG12PB7HN5W24AM2EOKIOM9KS-KERT>

You can use VOIP on your computer or dial-in using the phone number below.

Audio Connection

+1-415-655-0001

Access code: 194 196 960