Date – 3/30/2015
Attendees: CJ Clark, Adam Ley, Bill Tuthill, Bob Gottlieb, Brian Turmelle, Craig Stephan, Dharma Konda, Dwayne Burek, Frans de Jong, Gobinathan Athimolom, Jon Colburn, Josh Ferry, Marc Hutner, Mike Ricchetti, Steve Sunter, Tapan J Chakraborty,

Absent with Excuse:

Not present for ¾ of meeting:

Missing: Bill Huott, Carol Pyron, Jim Wilson, Kent Ng, Kevin Gorman, Tom Wayers, Heiko Ehrenburg, Dave Armstrong, Roger Sowada, Zahi Abuhanmdeh, Saman Adham, Teresa McLaurin, Philippe Lebourg, Gurgen Harutyunyan, Ismed Hartanto, John Braden,

Agenda:

1) Patent Slide
2) Steve to present latest slides
3) Craig to present his slides
4) Adjourn

Meeting Called to order at 11:00 am EST

Minutes:
Review Patent Slide – Slides Presented to the Group.
Solicited input from anybody who is aware of patents that might read on our standard.
No other responses noted.

Steve' presentation of slides on alignment
(Review of pdf's that Steve sent to reflector 3/25)

Craig gave a presentation on alignment
Standardize on 32 bits
Logic needed to align packet is small
Each SERDES has polynomial checker such that at speed SERDES BER can be performed.

Craig makes motion
Continue with the draft and implement 4 byte formatting for packets with 4 byte formatting of control characters. If it is found it doesn't work we can correct.

Brian Seconds motion.
(Steve questions if a motion and a second can come from the same company)

Josh Seconds motion. Wants to know though if we find it doesn't work can we change to correct?
CJ – always can make corrections

Discussion of Motion.
Steve – can we show its practicality? Would still like a block diagram showing the state machine.
Craig – There is nothing special about logic. It was implemented and logs are available from FPGA build as well as output from simulation.
Steve – could not come up with a straight forward circuit of everything. Concerned that DFT should be simple and straightforward to do it.
Tapan – estimate of how much overhead in either approach?
Craig – email provided LUTs in FPGA.
Bob – restriction is format will 4 byte format. Number of IDLEs must be 4 byte. But alignment can come at any point?
CJ – formatting is always on 32 bit boundaries.
Bob – IDLEs need to be in sets for 4 bytes?
CJ – yes.
Bob – not just variable
Steve – in Craig's IDLE is treated as own case. Control and data is another case
What I showed IDLE is a control character.
Bob – how does that ease the logic?
Steve – all it meant was that you have to do the crossbar at the beginning of the packet. After that everything was aligned.
Bob – if it is a 4 byte aligned packet.
Steve – when you look at the 4byte case it is all straightforward. Complexity was with larger cases. Problem is when you have a PHY that is larger than 4 bytes.
Bob – is the proposal restricting the size or can the implementation be whatever
CJ – the width of the PHY is whatever you need for the design.
For larger than 32 bits PHYs you would have quadrants.
128 byte PHY wouldn't matter. You would have a bigger chase statement.
Steve – Would like it known that he never said that 32 bits wouldn't work.
Tapan – if complex at higher size, maybe we can look at gate count or complexity at larger sizes.

Motion called

Yes

Bill T	Dharma K	Marc H
Brian T	Gobinatihan A	
Craig S	Josh F	

No

Bob C
Jon C

Abstain

Adam L	Steve S
Frans D	Tapan C

Motion **passes**

7 yes
2 no
4 abstain

Motion to adjourn: Craig
Seconded: Frans
Meeting adjourned: 12:00pm EST

Next Meeting:
April 6th, 2015 11:00am

Motion Summary

1 motion made

Continue with the draft and implement 4 byte formatting for packets with 4 byte formatting of control characters.

7 yes
2 no
4 abstain

Action Items

~~Bill Tuthill – 10-21-2013 -Add minutes and Attendance spreadsheet to the website.~~
~~CJ 11-11-2013 Reach out to ATE industry and Probe Industry to get update on future of ATE equipment to see which data speeds and protocols they are heading towards.~~
~~Philippe – Look into alternative method to create control information (pause, start, terminate, etc.) rather than using K characters in packet.~~
~~Bob – create a case study to show use of Attributes~~
~~Frans – will start some block diagrams of a simple use case to help illustrate the current architecture~~
~~Dwayne – present to the group his ideas for a simplified scheme – Direct Interface.~~
~~Adam – invite someone from IEEE to speak on IEEE benefits of standardization at WG meeting~~

Call for Essential Patent notes
Adam Ley 12/1/2014

PN, TTL, AN
7348796, METHOD AND SYSTEM FOR NETWORK-ON-CHIP AND OTHER INTEGRATED CIRCUIT ARCHITECTURES, DAFCA INC.

Steve Sunter 11/17/2014

1. US 7610532 “Serializer/de-serializer bus controller interface” Avago, granted 2009
2. US 7739567 “Utilizing serializer-deserializer transmit and receive pads for parallel scan test data” Avago, granted 2010
3. US 8543876 “Method and apparatus for serial scan test data delivery” Altera, granted 2014

NOTES:

1149.10 working group website - http://grouper.ieee.org/groups/1149/10/

Here is the WebEx conference link.

https://meetings.webex.com/collabs/meetings/join?uuid=MAG12PB7HN5W24AM2EOKIOM9KS-KERT

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