IEEE 1149.4 Mixed-Signal Test Bus Working Group Meeting Minutes

for
February 22nd, **2005**

8:00AM-10:15AM

Meeting Agenda:

Time	Topic	Responsibility
8:00 AM	1. Introduction and Review meeting minutes on October 20th, 2005 and November 7, 2006.	Bambang Suparjo
8:30–10:15 AM	2. Review the current status of ABSDL development. 3. Identify areas that need to be updated or developed. 4. Propose development plan/schedule for 2006.	All
10:15 AM	Meeting adjourned.	Bambang Suparjo

Meeting Attendees:

Name	Company
Adam Cron	Synopsys
Adam Ley	Asset-Intertech
Keith Lofstrom	Keith Lofstrom Integrated Circuits
Ken Parker	Agilent Technologies
Bambang Suparjo	Mentor Graphics

1. Introduction and Review the Meeting Minutes

1.1 Introduction

Two additional items have been added in the agenda:

a. Description of internal ABM by Keith.
b. Discussion regarding question from Philippe Lebourg, STMicroelectronics.

1.2 Meeting Minutes Approval

Adam Ley suggested the meeting minutes on October 20th, 2005 and November 7th, 2005 to be approved, and the group accepted the suggestion.

1.3 Action Items in Meeting Minutes October 20th, 2005.

a. Adam Ley mentioned there are several action items that have been assigned to him but not listed in minutes 1.3. The action items are:
   - Resolve safe value issue
   - Revise Kitchen Sink example
   - Revise Straw Dog example
   - Revise syntax BNF

b. Heiko has updated the semantic checks proposal.

1.4 Items in Meeting Minutes November 7th, 2005.

a. Election of Officers

Bambang requested more specific statement; Ken Parker nominated Bambang as the Chair, seconded by Adam Cron, and Adam Cron nominated Heiko as the Vice Chair.

b. Comments from the ABSDL proposal

- Ken requested information on the latest version of "Straw Dog" and "Kitchen Sink". The latest version of "Straw Dog" is 2_1 and "Kitchen Sink" is 2_2. Adam Ley will send the latest version to the group and Adam Cron will put them in the group website.

- The group will review why disable result for BIDIR shall be Z.

- The name MST_ABM_Pins is long. This item will be discussed in the next meeting.

- Bambang will send the NSC chip's pseudo BSDL (from Steve), to the group.

2. Review the current status of ABSDL development.

2.1. Standard Review

Bambang informed the group that the standard review deadline has been extended to December 2006. Bambang has communicated with Jodi Haasz, the Program Manager, International Stds Programs and Governance, on December 2, 2005 and confirmed the extension deadline is December 2006. The previous PAR (Project Authorization Request) application on P1149.4 (not 1149.4) has been withdrawn because it is not required at this stage. The group however is requested to apply for the PAR before the review deadline since ABSDL feature needs to be documented in the standard.

2.2. ABSDL Status

Based on the discussion, the current ABSDL should be able to perform extended interconnect test. There are few items need to be updated as mentioned in minutes 1.3 and 1.4b above.

3. Identify areas that need to be updated or developed.

Few items have been proposed by Heiko through email. Below are the items to be considered that are not listed in minutes 1.3 and 1.4b.

- Try to create an ABSDL file on the existing 1149.4 devices, for example STA400 from National Semiconductor, to verify its capabilities. Bambang will work on this.

- ABSDL may have to be extended to allow the description of additional features.

4. Propose development plan/schedule for 2006.

The group proposed to setup a monthly meeting on Wednesday, 8:00-10:00 AM, in the third week of each month. The next meeting will be on March 22nd, 2006. The group needs to setup special meeting to document ABSDL. The date will be determined later.

5. Description of internal ABM by Keith.

Keith presented the internal cell description shown in Appendix A. Ken raised a concern regarding the definition of full ABM and partial ABM where it requires modification in the documentation.

However, if the work that Keith is doing can detect the defect in power interconnection, Ken suggested to Keith to write a paper and demonstrate the standard application can be extended to provide such capability. Ken will inform people at Cisco on this possible feature.

Adam Ley commented the application is not currently documented in the standard. However, the documentation can be enhanced to include this application and describe the internal nodes and define the switch cells that associated to the internal nodes.

Adam Cron commented that current ABM can be used to implement this feature without the need for special requirement, but Ken pointed out that the number of boundary registers in a scan chain can be high when using the present ABM architecture. Separate instruction or scan chain may also be needed.

Ken would like to discuss this issue off line with other board test people.

As a conclusion, there will be no description on this specific application to be included in ABSDL.

6. Discussion regarding question from Philippe Lebourg, STMicroelectronics.

The email is shown in Appendix B.

Keith commented that there are 3 issues could be considered:

1. Will the approach interfere with the actual test?
2. Will this cause problem to the chip?
3. Will this meet the 1149.4 compliance?

Adam Ley commented that this is related to the construction and implementation of TBIC.

Adam Ley will review further this question and give the answer to Philippe.

Appendix A - Internal ABM cells / Keith Lofstrom, KLIC / Feb 22, 2006

ABMs on internal nodes are useful for chip level and board level testing. For example, a chip with multiple pins to a single power supply (say, 20 pins connected to VDD) needs all those connections properly soldered to the board to minimize proper voltage drops and noise levels in operation. A single unsoldered power supply pin can lead to intermittent failures that are difficult to detect with low speed digital-only testing. However, that same power supply pin (or an internal point on a bus connected to it) can be measured with an "observe only" ABM, and the extra millivolts of voltage drop can pinpoint a bad connection, leading to increased system-level reliability.

Other voltages unconnected to pins might need monitoring, such as the center tap of the terminating resistor of a digital receiver, for example. Unbalanced voltages on the center tap indicate that one of the two resistor segments has the wrong value, allowing testing of terminators even in situations where the driving impedances cannot be removed from the circuit.

There are of course many opportunities for internal chip measurement and control. It might be useful to yank on an internal node to see what an output pin does, perhaps increasing a biasing level to see if an analog driver output moves in an expected way.

There are two important kinds of internal ABM:

1) Full ABM with all switches
2) Observe-only ABM, using only switches SB1 and SB2

An internal ABM does not participate in simple interconnect test, and this distinguishes it from a pin-connected ABM. It is more likely to be used for other types of tests to be standardized in the future (for example, the center tap or power supply tests mentioned above). Bit settings for internal ABM cells should not change the behavior of simple interconnect tests on pins. It may change some biasing levels for extended voltage/current testing, so such cells will need specified "safe" states, or else characterization with residual elements.

An internal full ABM cell will have a core disconnect switch, will be drivable to VH, VL, and VG, and has a digitizing receiver. Even though it does not connect to the rest of the interconnect test network, these internal functions may can be useful for internal testing, or for putting the chip into a safe state for testing. For example, this could be used to put a feedback loop into a safe state when external portions of the loop are rendered unusable by simple interconnect test. This cell will have all the states specified in 1149.4-1999 table 6.

An observe-only ABM theoretically needs only two control bits for SB1 and SB2, but bits are cheap, and an additional bit pattern may complicate the task for software writers (PLEASE VERIFY). An observe-only ABM should have all 4 bits, with two of the bits having no measurable effect, and optionally set to 00 as a safestate. The states in table 6 that are actually implemented will be p16 through p19; all the other states will map onto this state for this observe-only ABM. These states are not directly observable during simple interconnect test.

Appendix B – Email from Philippe Lebourg

From: Philippe LEBOURG [mailto:philippe.lebourg@st.com]
Sent: Mon 02/13/2006 9:28 AM
To: Suparjo, Bambang
Cc: stds-1149-4wg@mail.ieee.org
Subject: Re: 1149.4 Meeting

Hi!

I've been following this work group's mail exchange for a while and I find you did a great job! The last sending (absdl_05_edit.pdf) is clear, concise and shows powerful possibilities. Congratulations!

I still have a question regarding this last sending: is it possible in the current definition of ABSDL to use a same pad both as an ATAP1N pin and as an ATAP2 pin?

I'm not asking this just out of pure curiosity but because our imagers currently have two ATAP pins (not yet controlled through IEEE 1149, alas! :) but these are currently being used for both types of operation. It would be quite annoying for us to have to define one additional ATAP pin (where to bond it? No room!) or to have to move ATAP2 functions to ATAP1 one (not possible in every configuration type anyway, and probably not wished by the engineers in charge of debug!). NB: This is so because the differential stuff is quite a marginal one.

Thanks in advance for your reply.
Philippe LEBOURG
STMicroelectronics 04 76 58 6422