

AC EXTEST Preliminary Specification

Prepared by the AC EXTEST Working Group

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Abstract: This standard augments IEEE 1149.1 to improve the ability for testing differential and/or AC coupled interconnections between Integrated Circuits on boards and systems.

Keywords: AC Coupled Signals, Boundary-Scan, Differential Signaling, Interconnect Testing

Introduction

(This introduction is not part of this standard.)

The development of this standard was begun May 21, 2001 by an ad-hoc industry Working Group called by Agilent Technologies and Cisco Systems. This group formulated this draft standard, with the intention of handing it over to the IEEE for formal standardization when the underlying technology became understood.

The group adopted as its mission:

To define, document and promote a means for designing ICs that support robust Boundary-Scan testing of boards where signal pathways make use of differential signaling and/or AC coupled technologies. This technology utilizes and is compatible with the existing IEEE 1149.1 standard. The goal is to upgrade the capabilities of IEEE Std 1149.1-2001 to maintain the rapid and accurate detection and diagnosis of interconnection defects in boards and systems despite the fault masking effects of differential signaling and the DC blocking effects of AC coupled signaling.

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1 Overview

1.1 Scope

This document describes the details of a solution for testing differential and/or AC-coupled nets between integrated circuits on printed circuit boards or in systems. Traditionally, such interconnect has been DC-coupled and can thus be tested with well-known Boundary-Scan methods, specifically with the EXTEST instruction as codified in IEEE Std 1149.1-2001. However, the use of AC-coupling technology disallows DC-based techniques, and differential signaling can cause fault masking effects, giving rise to the need for an extension of Boundary-Scan into the AC and differential realms.

1.2 Organization of the Standard

Clause 1 provides an overview and context for this standard.

Clause 2 provides references necessary to understand this standard.

Clause 3 defines terminology used in this standard.

Clause 4 outlines the technologies addressed and utilized by this standard.

Clause 5 discusses the on-chip resources needed for testing.

Clause 6 provides rules for implementation.

Clause 7 provides rules for conformance and documentation of devices designed to this standard.

Clause 8 shows how this standard is used in typical testing applications.

1.3 Context

Figure 1 shows a printed circuit board containing many types of devices. Of these, some could be compliant with IEEE Std 1149.1 for the support of testing activities. These devices contain Boundary-Scan testability circuitry which allows them to participate in manufacturing tests that detect and diagnose faults such as open solder joints, shorts and missing devices.

The additional testability elements added by this standard to these same ICs allow this interconnect testing to be conducted on differential signal pathways and/or where AC coupling (which blocks normal DC test signals) has been used on signal paths between ICs.

1.4 Objectives

The objective of this standard is to provide design guidance for additional testability circuitry added to an IC already compliant with IEEE Std 1149.1-2001 such that when such an IC contains differential signaling and/or is AC coupled with other ICs compliant to this standard, board and system level tests can be readily and accurately conducted.

Devices that adhere to this standard that are used in differential and/or AC coupled signaling environments will realize significant savings in testing costs for boards and systems. Tools that are cognizant of the capabilities provided by this standard will be able to prepare, run and interpret these tests in a highly automated fashion, with high diagnostic resolution.

This standard allows devices created by multiple vendors to operate together during testing despite the differing characteristics and parameters of the IC processes used to fabricate the devices.

This standard also provides design guidance to board and system designers that will enhance the performance of the testability features of their products. This in turn will reduce system and production costs.

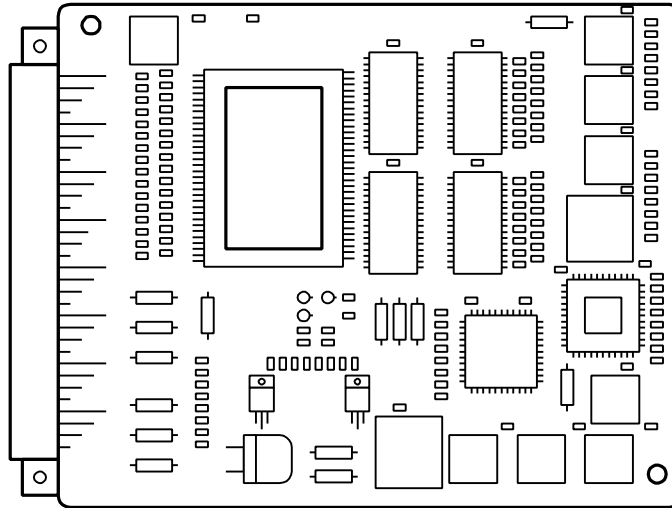


Figure 1: A printed circuit board containing a variety of components interconnected by printed wiring. Some ICs contain IEEE 1149.1 features that support Boundary-Scan interconnect testing.

2 References

This document shall be used in conjunction with the following standards. When the following standards are superseded by an approved revision, the revision shall apply.

IEEE Std 100-1996, IEEE Standard Dictionary of Electrical and Electronic Terms.

IEEE Std 1149.4-1999 IEEE Standard for a Mixed Signal Test Bus.

IEEE Std 1149.1-2001, IEEE Standard Test Access Port and Boundary-Scan Architecture.

3 Definitions and Acronyms

3.1 Definitions

- AC Coupling:** The use of series capacitance in a signal path. This coupling will block DC voltages on the drive side of the path from appearing on the receive side. Only the AC component of the driven signal will pass through the coupling, with the effect of high-pass filtering imposed on the original signal. *Contrast with **DC coupling**.*
- Bias:** A high impedance (typically >1000 ohms) voltage source often used on the input of a receiver to cause it to output a deterministic state in the absence of an input signal.
- Bias network:** A network of impedances, usually higher-valued than termination impedances, used to establish a common mode or reference voltage.
- Channel:** A **signal path** or set of signal paths that transmits a single data stream from a source to a destination. *See **differential signaling** and **single-ended signaling**.*
- Characteristic Impedance:** the ratio of the complex voltage and complex current of a signal traveling forward on a conductive path.
- Common mode noise:** A noise signal added equally to both signal paths in a differential signal channel.
- Common mode range:** The range of common mode voltage that a differential receiver is capable receiving while maintaining reliable signal recovery. A differential signal with common mode voltage within this range will be received correctly. Outside this range the receiver may fail to recover the data signal.
- Common mode voltage:** The voltage at which a differential pair of signals is designed to cross over (i.e., their difference is zero), in the absence of noise.
- Comparator:** An amplifier with two inputs labeled positive and negative, typically with very high input impedance. The amplifier usually has very high gain and produces an output signal that is the amplified difference of the positive and negative input signals. For all but the smallest differences, the output will be $V_{\max}$ or $V_{\min}$, which are the most positive and most negative voltages the amplifier can produce on its output. A comparator can be used as a differential receiver. A comparator can be used to determine if an input signal is logically above or below a reference voltage.
- Current signaling:** A signal encoded by the amplitude and direction of current flow. In a differential pair, a current signal is positive when current flows from positive to negative legs, and negative in the reverse direction. The voltage that may appear on these same legs does not carry information. *Contrast with **voltage signaling**.*
- DC Coupling:** The use of simple wires or small series resistances in a signal path. *Contrast with **AC coupling**.*

Derived voltage reference: a voltage reference derived: 1) from other references, such as a resistive divider between power and ground, or 2) a resistive divider between two differential signals that recovers the common mode voltage of the signals.

Differential driver: A driver that accepts a single data stream and drives it onto two independent signal paths where one signal is the inverse of the other. The two signals are centered at the common mode voltage.

Differential receiver: A receiver that recovers a single data stream encoded differentially on two signal paths. It effectively subtracts the signal on its negative leg from that on its positive leg. This eliminates **common mode noise** appearing on both legs.

Differential signaling: The use of two independent signal paths in a channel to carry a single data signal, where one path carries an inverted copy of the signal that appears on the other path. The original data signal can be reconstructed by taking the difference of the two signals and there is no reliance on a reference voltage for determining this signal. This has the property of eliminating **common mode noise** in the transmitted signal. *Contrast with single-ended signaling.*

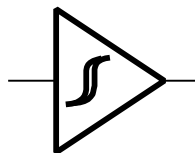
Frequency: The number (f) of transition pairs that occur on a signal path in one second. With respect to **AC Coupling**, a frequency is **high** when the period ($1/f$) is small compared to the **time constant** of the coupling. A frequency is **low** when the period is large compared to the time constant of the coupling.

Float: The state of an input to a receiver that is not connected to a signal, or a high impedance connection to a receiver input.

High pass filter: An electrical network that passes higher frequencies and attenuates lower frequencies. DC current is blocked.

Hysteresis: From magnetics: lagging in the values of resulting magnetization in a magnetic material (such as iron) subjected to a changing magnetizing force. In this document, hysteresis refers to the memory of an input state to an amplifier or buffer after that state is removed but before a different input state is applied. Typically there is a hysteresis threshold that defines the difference between “no input” and “input.” As applied to electronics, a digital output circuit such as a comparator where the output switches to one output state when the input is above one level and switches to the opposite output state when the input is below a lower level, and the output does not switch at any intermediate level. Example: a buffer produces a high output when a voltage above 0.5 volts is applied, produces a low output when a voltage below 0.3 volts is applied, and does not change its output for voltages between 0.3 and 0.5 volts.

Hysteresis symbol in a buffer symbol:



Hysteretic:	Adjective form of hysteresis , as in “hysteretic amplifier.”
Interconnect test:	An IEEE Std 1149.1 Boundary-Scan test designed to detect and diagnose defects in the interconnection wiring between ICs. This standard extends the concept to include the testing of channels, where single-ended and differential signaling, and DC or AC coupling may exist.
Low pass filter:	An electrical network that passes lower frequencies, including DC levels, and attenuates higher frequencies.
Mission logic:	The circuitry inside an IC that performs its primary design function. <i>See test logic.</i>
Mission mode:	A device or pin of a device performing its primary design function. <i>Contrast with test mode.</i>
Negative leg:	The signal path of a differential signal pair that has the opposite polarity as the original data signal.
Null:	The input state where the two inputs to a differential receiver which are supposed to be different (complementary) are instead receiving the same value.
Offset voltage:	A constant DC voltage added to an AC signal.
Operational modes:	A pin may operate in one of two modes, “mission” and “test” mode. <i>See mission mode and test mode.</i>
Positive leg:	The signal path of a differential signal pair that has the same polarity as the original data signal.
Reference voltage:	A low impedance voltage source typically used to define a threshold for comparing signals. The low impedance characteristic means it is resistant to conducting noise signals.
Referenced termination:	A termination for a differential channel where the two legs are both terminated to a reference voltage.
Self-referenced comparison:	The comparison of a signal with a delayed version of the same signal, used to detect signal transitions. This process does not need a static reference voltage to find a transition in a signal.
Signal Path:	An electrical pathway formed by a simple conductor, or a terminated pathway containing a series resistance, or an AC coupled pathway containing a series capacitance, that transmits a signal from a driver to a receiver.
Single-ended signaling:	The use of a single signal path in a channel to carry a data signal. The signal is referenced to a static reference voltage. <i>Contrast with differential signaling.</i>
Slew rate:	Rate of change in either direction of voltage in a specified time, measured in units of volts per second.
Termination:	An impedance usually near the end of a signal path used to satisfy the electrical matching requirements of the characteristic impedance of the signal path. The impedance is typically low, often 100 ohms or less. <i>See also characteristic impedance, referenced termination and unreferenced termination.</i>

Test logic:	Testability logic defined by this standard and IEEE Std 1149.1. <i>Contrast with mission logic.</i>
Test mode:	A device or pin of a device that, in response to the EXTEST or AC_EXTEST instruction, is now driving and/or receiving test data as controlled by the test logic of the IC. It has been disconnected from the internal mission logic of the IC. <i>Contrast with mission mode.</i>
Time constant:	Typically the product of resistance and capacitance of an RC network (e.g., a high pass filter) measured in seconds. One time constant is the time for a capacitor to discharge 63% of its voltage through a resistor. In AC coupled systems, the termination resistance combined with the coupling capacitor forms a high pass filter. (See high pass filter .)
Transition:	A voltage transition occurs when a signal traverses a specified voltage range in a specified time in either direction. See slew rate .
Unreferenced termination:	A termination for a differential channel where a termination impedance is connected between the two legs with no connection to a reference voltage.
Voltage signaling:	Signals are encoded by the voltage appearing on a wire compared to a reference voltage (single-ended) or the voltage appearing on a pair of wires (differential). <i>Contrast with current signaling.</i>

3.2 Acronyms

CML:	Current mode logic
HSTL:	High-Speed Transceiver Logic
LVDS:	Low Voltage Differential Signaling
LVPECL:	Low voltage PECL (Pseudo Emitter Coupled Logic)
PECL:	Pseudo Emitter Coupled Logic
TAP:	Test Access Port (from IEEE Std 1149.1).

4 Technology

The presence of coupling capacitors on chip interconnects, whether they are discreet devices mounted on a PC board or integrated inside an IC, prevents DC values from being driven between chips. An AC Boundary-Scan methodology must therefore use a time-varying signal to pass through the AC coupling when in AC EXTEST mode.

Differential signaling is often used to increase signaling speeds and noise immunity, compared to single-ended coupling. Differential signaling, combined with termination schemes, can have significant defect masking properties that reduce test effectiveness.

4.1 Signal Pin Types

It is expected that a chip possessing pins requiring AC coupling will also possess “normal” (i.e, DC coupled) pins as well. These DC pins would supply data and/or control to/from portions of the chip that do not require AC coupling. For test purposes, it is necessary that all these pins be tested simultaneously with an EXTEST-like capability because that is how shorts (unwanted connectivity) between these pins are reliably detected. This document will refer to DC and AC pins henceforth. DC pins are those that IEEE Std 1149.1 currently governs for testing. AC pins have been treated by 1149.1 as an “analog” problem and effectively ignored.

AC pins are a principle target of this standard. IC designers implementing this standard are expected to identify such pins and add new test capabilities for them.

4.2 Signal Coupling and Coupling Combinations

This section reviews a range of coupling options.

4.2.1 Single-ended DC

A basic, single-ended connection scheme is shown in Figure 2, along with the Boundary-Scan control and observation capability specified by IEEE Std 1149.1. This type of coupling has been quite common and is very testable using Boundary-Scan.

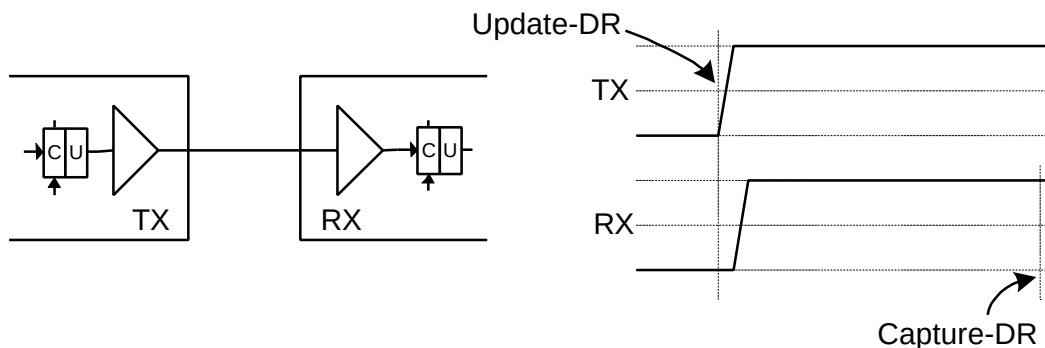


Figure 2: Basic single-ended signaling with Boundary-Scan control and observation.

4.2.2 Single-ended AC

Figure 3 shows an AC coupled single-ended connection. (The termination resistor and voltage source shown may not be necessary thus would be omitted .) While the devices may have been designed for DC coupling and actually contain Boundary-Scan resources, the AC coupling will

block their operation. This interconnection configuration is thus untestable with standard Boundary-Scan algorithms. This is due to Boundary-Scan test data rates being relatively low since they are a function of the test clock (TCK) rate which may be significantly lower than the normal operating frequency of the channel being tested. The data seen by the receiver will decay before it can be captured.

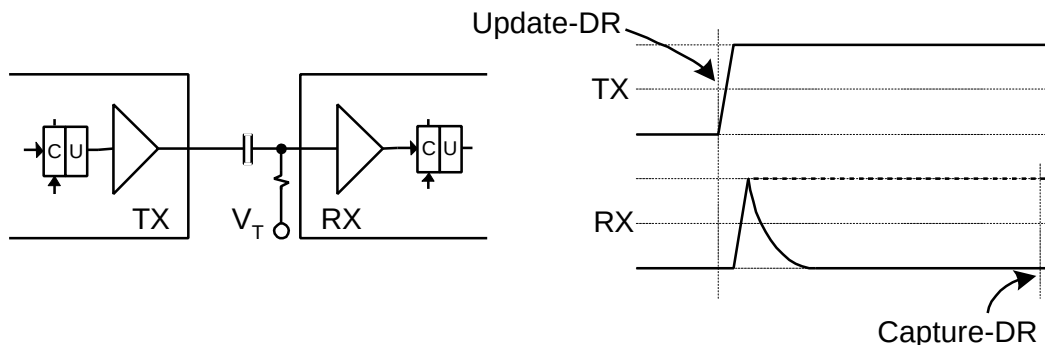


Figure 3: Basic single-ended signaling with AC coupling.

4.2.3 Differential DC

Figure 4 shows a basic differential DC coupled signal path. The termination resistor may exist for impedance matching and/or source termination of the driver. The placement of Boundary-Scan resources is optional per IEEE Std 1149.1 in that they can be omitted altogether. The 1149.1 standard allows a designer to designate the differential signal path as “analog”. Then the digital-to-analog and analog-to-digital interfaces (optionally) can be provided with Boundary-Scan resources as shown in Figure 4. When this option is taken, it is then possible to test the “analog” signal path with Boundary-Scan algorithms.

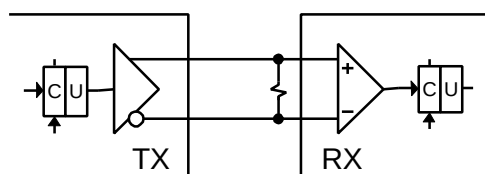


Figure 4: Basic differential signaling with DC coupling.

The driver in Figure 4 could be producing a voltage signal and the resistor is used to match the signal line impedance. Alternatively, the driver could be producing a current signal, where the direction of flow represents data, and the resistor is needed not only to match signal line impedance, but also to provide a DC current path to satisfy the driver’s requirements. This is called a source termination.

4.2.4 Differential AC

Figure 5 shows AC coupling of a voltage driver and receiver that could be completely incompatible for DC coupling because the voltage levels used by the driver are too far removed from the acceptable common mode range of the receiver. The termination network referenced to the common mode voltage source V_T , along with the DC blocking effect of the coupling capacitors, allows this configuration to work properly. This enforced compatibility is a common reason why board designers may use AC coupling.

NOTE – The receiver waveforms in Figure 5 will decay to V_T if the driver frequency is low compared to the time constant of the coupling network. Since Boundary-Scan test data application rates can be low, the receiver may indeed see null levels due to signal decay.

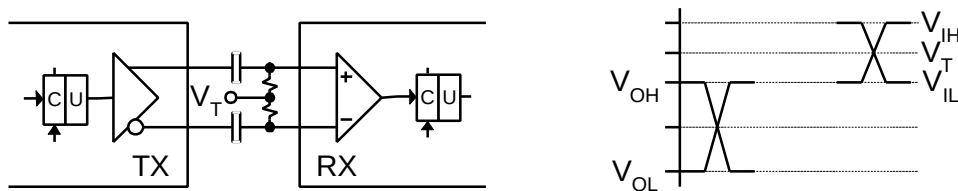


Figure 5: A basic differential AC signal path with referenced termination and common mode generation.

Figure 6 shows a basic differential AC signal path with an unreferenced termination. The termination is used for impedance matching.

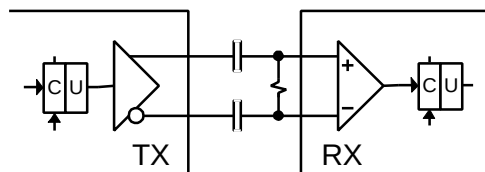


Figure 6: A basic differential AC signal path with unreferenced termination.

Figure 7 shows a basic differential AC signal path with a current driver and source termination, and also a referenced bias generator to select the common mode voltage appropriate for the receiver. The source termination may also serve as an impedance match for the line. The bias network may use significantly larger resistors as long as the line distance from the capacitors to the receiver is small. This will significantly increase the time constant of the coupling network.

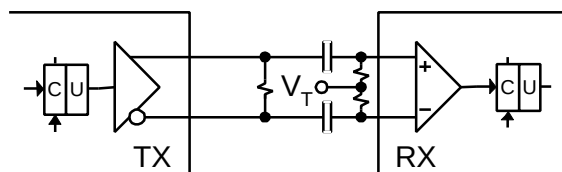


Figure 7: Basic differential AC signal path with source termination and bias provision.

Finally, all the terminations, bias networks and even the coupling capacitors may ultimately be integrated into the receiver IC. Externally, the signal path appears to be DC coupled but internally it is still AC coupled, as shown in Figure 8.

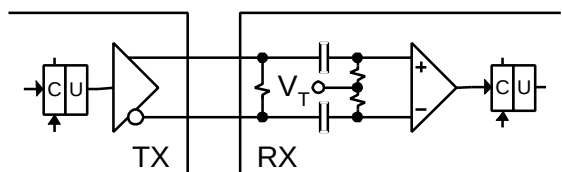


Figure 8: AC coupling, termination and bias generation internal to the receiver.

4.2.5 Intention: When AC Capability Is DC Coupled

The standard for AC EXTEST proposed herein is intended to be implemented on AC pins of an IC. However, there is the possibility that a board designer may still choose to use DC coupling between devices that are DC compatible. Thus a test developer could find a situation where AC EXTEST is needed to test a DC coupled signal path. This could occur when more than one AC-capable interface exists on an IC and one is AC coupled while another is DC coupled. The test developer would need to load the AC EXTEST instruction into the device to test the AC coupled interface. It is the intention of this standard that if DC coupling of AC-capable interface is possible and gives acceptable mission performance, then the AC EXTEST test performance will also be acceptable.

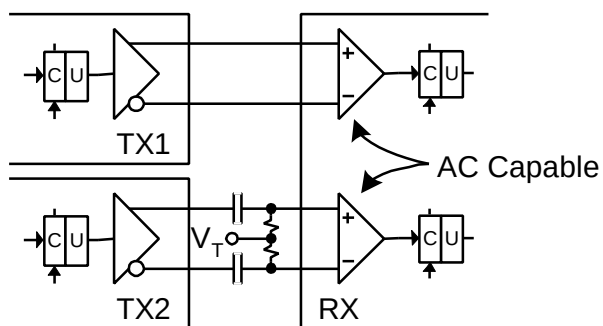


Figure 9: An AC-capable receiver connected to an AC-capable driver and a conventional driver.

For example, in Figure 9 a conventional IC (TX1, containing only EXTEST support) is DC coupled to a receiver in RX. An AC-capable driver TX2 is also connected to the receiving IC. To test all the signal paths simultaneously, the conventional device TX1 must be in EXTEST while the other two use the AC EXTEST instruction.

4.3 The Effects of Defects

Defects are abnormalities in the structure of a board that occur during manufacturing that must be found and corrected. This “manufacturing defect” model includes things like open solder joints, shorts, missing components and dead devices. Not included in this model are performance-related issues, for example, the failure of a device to operate at its highest specified frequency. This recognizes the traditional role of IEEE 1149.1 as a test standard for manufacturing defects.

The advent of AC coupling, especially in the differential signaling domain, threatens this role. There is inherent redundancy in differential structures that can mask the presence of seemingly obvious defects. An example is shown in Figure 10.

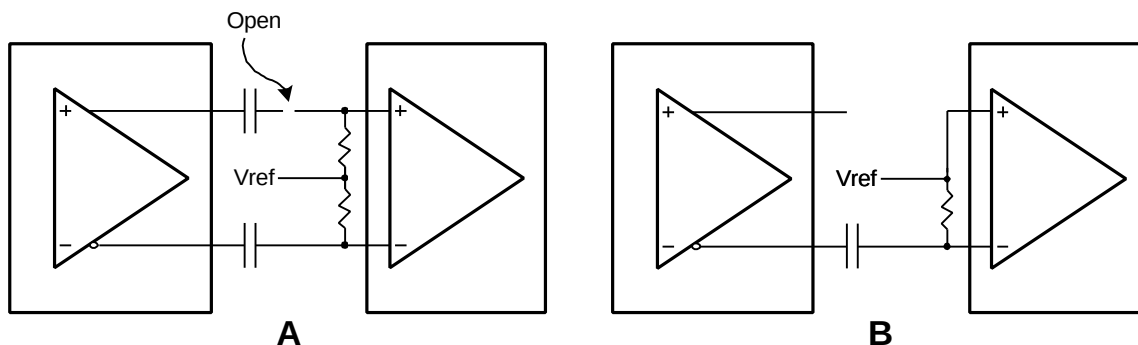


Figure 10: An AC coupled differential path containing a defect (A) and an equivalent circuit (B).

In this case, the positive leg of the circuit is eliminated by a defect, for example, an open solder joint on the capacitor. Yet the receiver still receives the negative leg signal and compares it to the V_{ref} voltage. The receiver will still produce the correct output, although its common mode noise rejection capability is completely compromised. This might not be noticed until subsequent functional or performance testing is encountered. There it may show up as an elevated bit error rate which would not provide very much diagnostic information. This simple example illustrates why it is important to monitor *both* legs of a differential pair, as covered in section 4.5.4.

One defect in particular may be troublesome to detect in AC coupled structures: the shorted capacitor. This defect restores DC coupling. This defect may go unnoticed particularly in differential signal paths, especially when the DC characteristics of the driver and receiver are similar. For this reason, it is important to support the standard EXTEST instruction, because it

can be used to test for shorted capacitor defects. This can be done by supplying a stream of 0s and 1s to the driver side of the capacitor and showing that this stream does not show up on the receive side.

Finally, it is important to realize that defects that occur in high-speed circuits (where slew rates are often faster than signal path transmission times) there may be transmission lines that affect the circuit's faulty behavior as shown in Figure 11. Simulation of the circuit's behavior may be necessary to understand the effects of defects. It is important to consider transmission lines as components of the simulated model when slew rates are elevated.

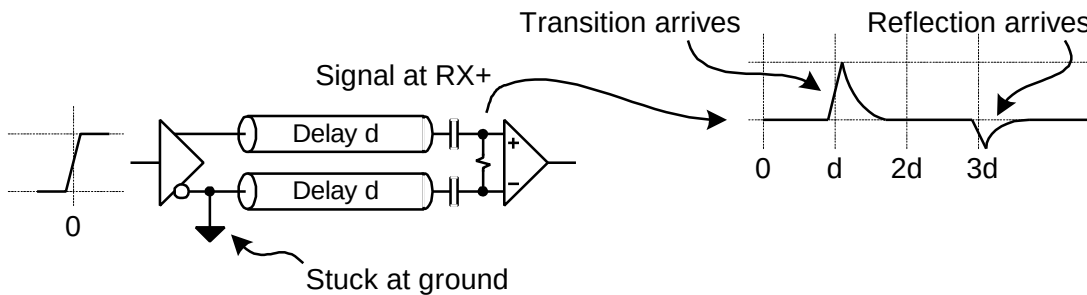


Figure 11: A defect may interact with transmission lines to produce unexpected effects.

4.4 Differential Termination and Testability

Extensive study of differential channels and the effects of defects within those channels has shown that the effects of defects are heavily influenced by the termination schemes used. There are three functions of terminations:

- to provide for proper DC paths needed for proper driver functioning, called “source termination”,
- to provide impedance matching of transmission lines, and
- in some AC coupled cases, to set common mode operating points for the receiver.

A given termination may provide one or both of these functions. The following subsections discuss termination options.

4.4.1 Unreferenced Termination

Source termination is usually needed for current signaling technologies, where the direction of current flow is used to encode binary data. A typical example is a Low Voltage Differential Signaling (LVDS) driver/receiver pair. Since all differential receivers operate by comparing voltages, a current signal is translated into a voltage signal for that comparison. Figure 12 shows an LVDS driver DC coupled to a voltage receiver, where R_S provides both source termination and impedance matching. The direction of current flow represents data.

NOTE – It is assumed that R_S is placed very close to the receiver so that any transmission line effects are only present between the driver and the resistor.

This form of termination is called unreferenced because there is a single resistor R_S rather than two resistors center tapped to a reference voltage (seen later in Figure 14). In effect, the receiver is referenced to the common mode voltage of the driver/resistor combination. This means the receiver's common mode range must be compatible with the driver's output.

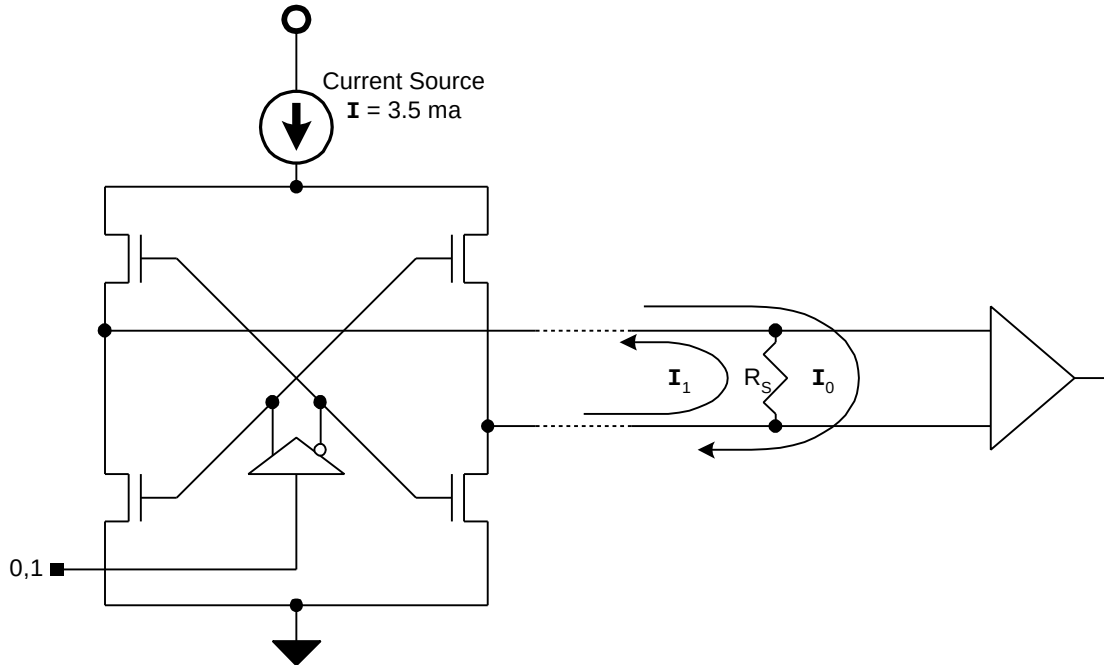


Figure 12: LVDS driver and receiver, DC coupled.

Figure 13 shows an un referenced AC termination. Resistor R_S still provides source and line termination. Resistor R_T provides a current path on the receive side, since the comparator input impedance is effectively infinity. Note R_T and C determine the time constant of this coupling.

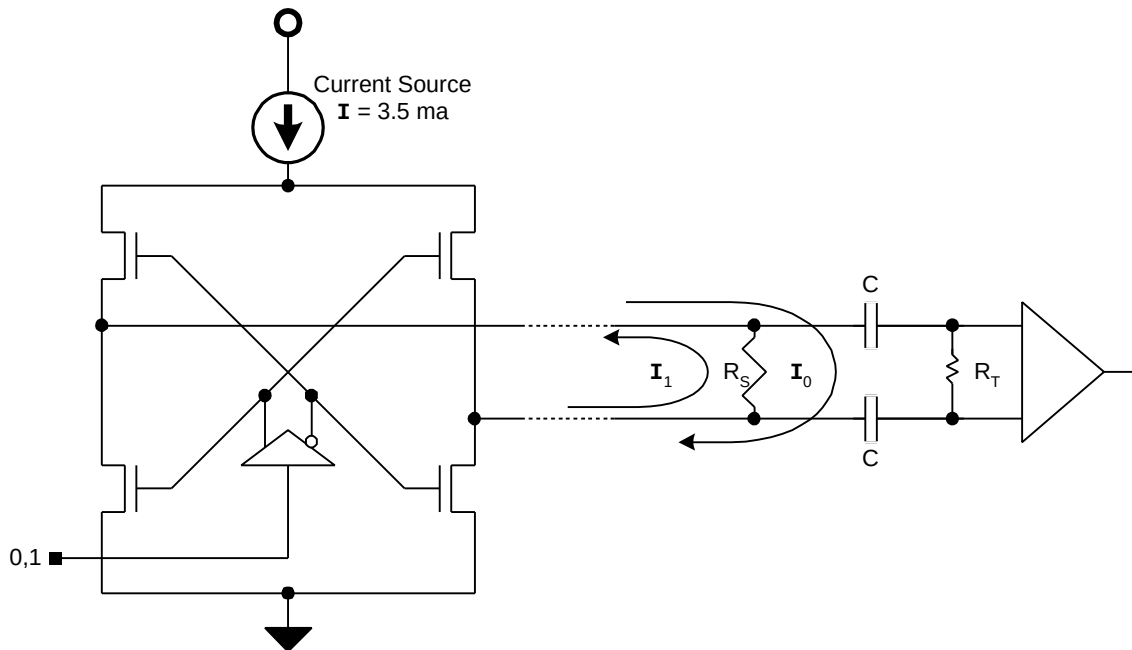


Figure 13: LVDS driver and receiver, AC coupled with un referenced termination on the receive side.

If the time between signal transitions is long, the voltage across R_T will decay to zero volts, or a null input condition with results that may be undefined. Note that some defects can also cause this to occur, such as either capacitor C missing. A null input condition during testing is undesirable due to its non-determinism. Because of this, un referenced termination is not preferred even though it saves one resistor.

4.4.2 Referenced Termination

Figure 14 shows an AC coupled, referenced termination. This type of termination is used to set the common mode voltage of the receiver at its optimal value (here, V_T). Resistors R_B along with capacitance C determine the time constant of the coupling.

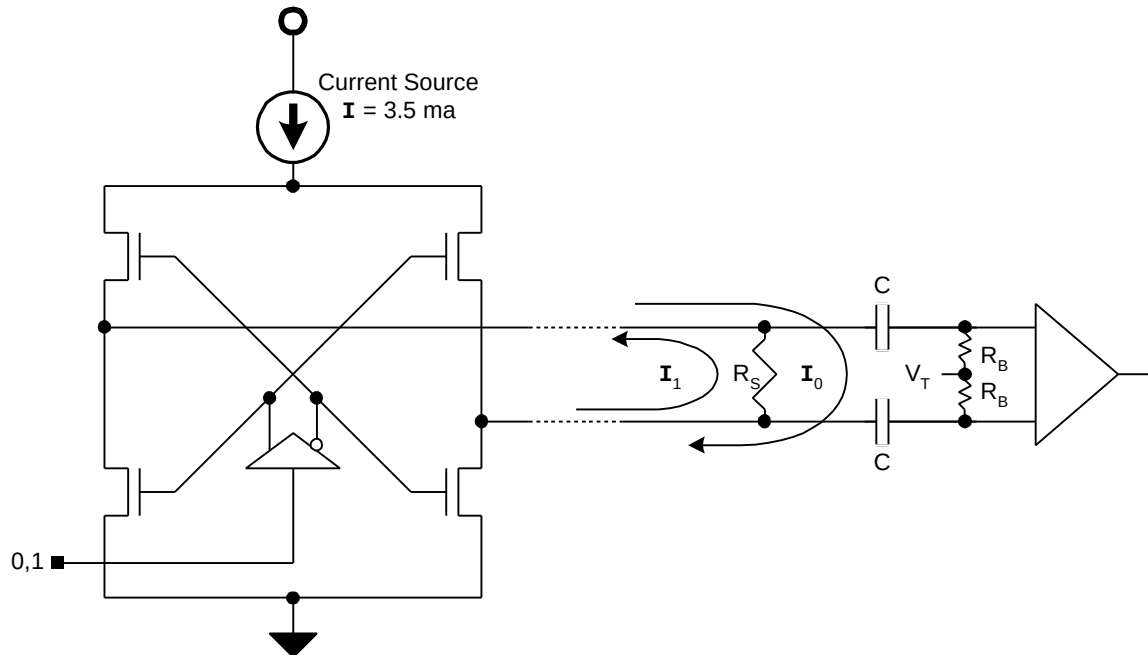


Figure 14: LVDS driver and receiver, AC coupled with referenced termination on the receive side.

In the referenced termination case, if a defect such as a missing capacitor is present (this defect is shown in Figure 10) both legs of the receiver will see deterministic voltages (no null condition). Since test structures are to be added to both legs (see 4.5.4) they will respond in a deterministic way. This is the preferred behavior of an AC coupled link.

4.5 Test Signal Implementation

In order to test the various combinations of single-ended and differential signal paths with variations on coupling, modifications have to be made to the drive and receive sides of the path.

4.5.1 Single-ended Drive

Figure 15 shows a single-ended output stage modified in the familiar way given by IEEE Std 1149.1 for test purposes. One of two signals, the normal mission signal or a test signal are selected for transmission by a test mode signal. (This figure does not show the full detail of the Boundary-Scan register cells that supply test data.) The concept here is that the single-ended driver itself is not modified.

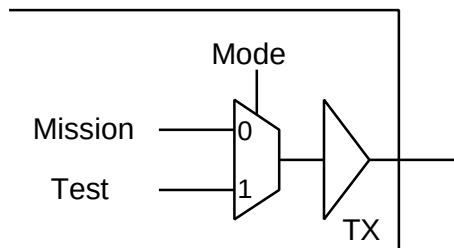


Figure 15: A single-ended driver path.

4.5.2 Differential Drive

There are two options for implementing a differential driver when incorporating test. The first is shown in Figure 16 where the selection between test and mission data is performed before the conversion to differential signaling. This means there will be only one data stream presented to the two differential pins and that the data will be transmitted in true differential form, using either current or voltage modes of the driver in question. Due to aggressive performance requirements in some higher-speed driver designs, it is expected that this option will often be chosen.

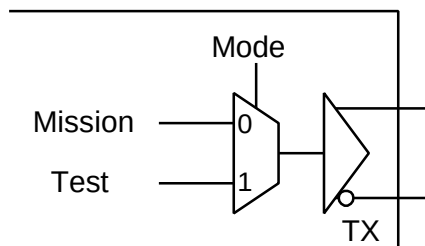


Figure 16: Full differential driver for both mission and test modes.

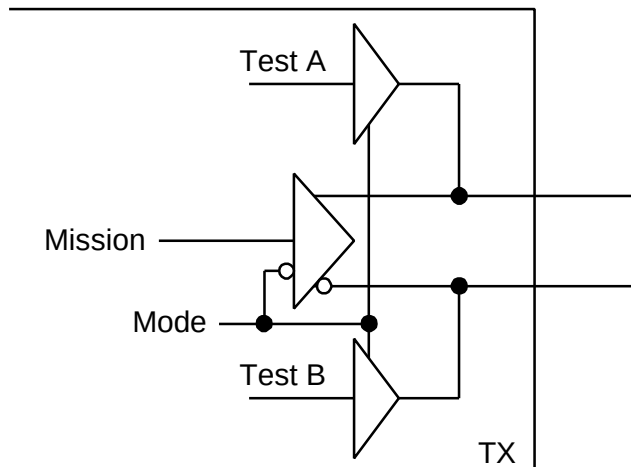


Figure 17: Differential mission/Single-ended test mode driver.

A second option for implementing testability in a differential driver is shown in Figure 17. In this case the mission mode signal path is differential, while in test mode the mission driver is disabled and two single-ended drivers with independent test data sources are enabled. Each controls a single side of the differential signal path. During test, the path is now a pair of independent single-ended signals. The two new single-ended test drivers must have similar drive characteristics as the mission driver to assure they are compatible with the loading and coupling that the mission driver would encounter.

NOTE 1 – In describing this case in BSDL (see section 7.2) the *test mode* of the driver signals are described which are single ended. Thus the signal pair is *not* described as differential. (See the “Grouped Port Identification” section B.8.8 in IEEE Std 1149.1-2001.)

NOTE 2 – If such a device supports IEEE Std 1149.4, then the structure in Figure 17 may be implemented, but with drivers of insufficient drive capacity to drive the load impedance. In this case, a hybrid of Figure 16 and Figure 17 may be implemented where AC EXTEST operates using the model in Figure 16.

This option has desirable testability and diagnosability features in that it removes some of the redundancy inherent in differential signaling, but it also reduces some of the noise immunity that differential signaling affords and may generate more noise during testing since the test signals on the two legs are no longer balanced and offsetting. There is additional cost in that the drive specifications (slew rate and amplitude) for the two added drivers must be substantially similar to those of the mission driver, into the mission load.

4.5.3 Single-ended Test Signal Reception

Figure 18 shows two options for single-ended test signal reception, again familiar from IEEE Std 1149.1, but with a provision for detecting an AC test signal when the AC EXTEST instruction is loaded in the device. (When EXTEST is loaded, the detector passes the received signal intact.) One option supports INTEST (control and observe capability) and the other uses a simpler observe-only structure that will not support INTEST.

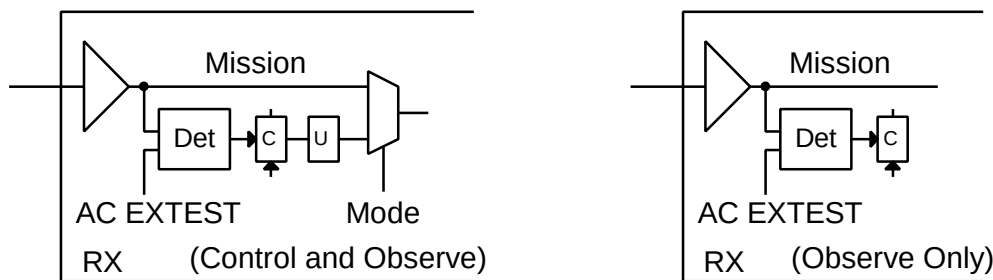


Figure 18: Choices for single-ended signal reception.

A single-ended receiver has some form of reference used to distinguish a ‘0’ from a ‘1’ and this feature is used during test as well. Thus the front end of the receiver (typically an ‘analog’ design) need not differentiate mission signals from test signals.

4.5.4 Differential Test Signal Reception

A differential receiver is modified for testability as shown in Figure 19. The mission differential receiver path is modified to capture test data seen by the mission receiver in differential mode. The mission receiver itself is unmodified.

NOTE – As shown, the mission receiver path would support INTEST, but an observe-only structure can be used instead if INTEST is not supported.

Each leg of the differential signal path has its own added test receiver. The purpose of this receiver is to monitor a leg of the signal path independently. This gives additional defect detection and diagnosis capability.

NOTE – No variations in the test receiver are needed for INTEST support since this is an observe-only monitor.

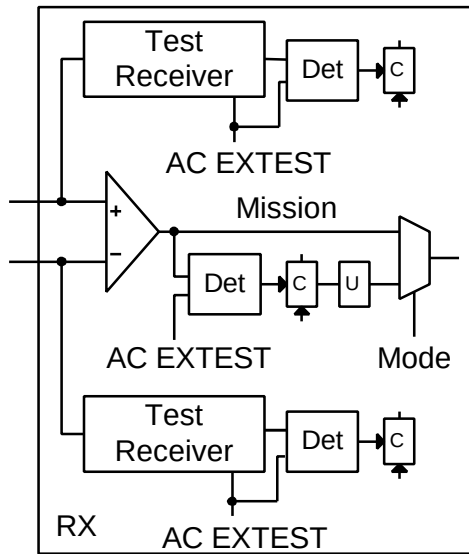


Figure 19: Differential signal reception.

Since the signals on the differential pair may contain a significant common mode offset as well as the test signal, the design of the test receiver must account for the fact that there is no fixed reference available to discriminate a '0' from a '1'. A general discussion of the test receiver is given in sections 0 through 4.8, and rules for its implementation are given in section 6.5.

4.6 Test Receiver Support for the AC EXTEST Instruction

The principle purpose of the test receiver seen in Figure 19 is to extract a test signal from one half of a differential pair of signals that may contain a common mode offset. Because of the common mode offset, a simple comparison of the test signal to a static reference may not reliably extract the test signal. Using the opposite leg of the pair as a reference (as is done by the mission receiver) will often mask many important defects. A solution is to look for information contained in the *transitions* of the signal. These will be independent of common mode offsets as shown in Figure 20. Valid transitions have a defined voltage swing ΔV and slew rate Δt .

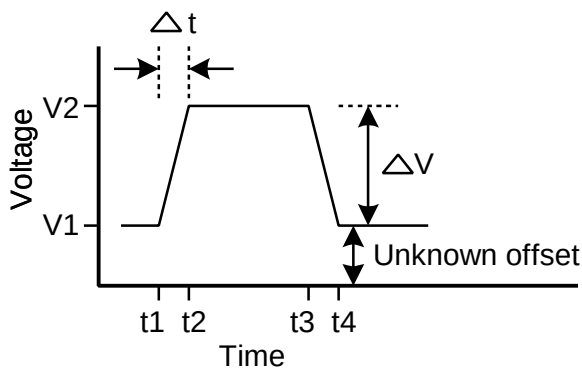


Figure 20: A signal with unknown voltage offset and the transitions it contains.

One way to find the transitions in a signal with an unknown offset is to compare the signal with a delayed version of itself, that is, to use its recent history as a reference. This is diagrammed in Figure 21. The original signal, a delayed version and the output of the hysteretic comparator are shown. The output is a faithful reconstruction of the original waveform, delayed by the time it

takes for the input waveform to pass the hysteresis threshold. The output waveform has been converted to standard logic levels, that is, the unknown offset is removed.

It will be important to assure that the delay D is longer than the transition times to be sensed. The use of hysteresis can eliminate unwanted response to small signal noise (run pulses). Additional filtering in the design of the comparator can eliminate response to larger signal noise of insufficient duration (noise spikes).

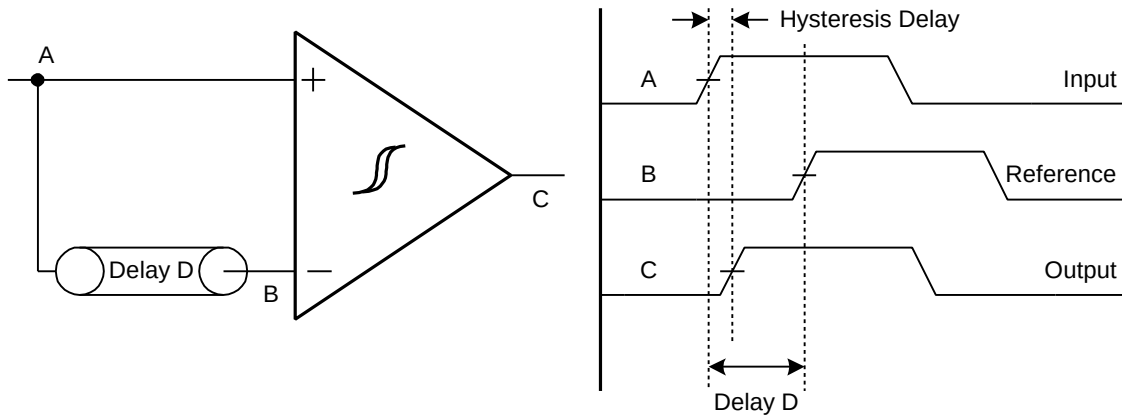


Figure 21: Delayed self-referenced reconstruction of an input waveform with unknown voltage offset.

Figure 22 shows a potential implementation of the concept shown in Figure 21. There are two simple comparators, one to sense rising edges and the other to sense falling edges. The V_{Hyst} voltage sources set the hysteresis point for the comparators. The comparator outputs set or clear a D-type flip-flop. The values of R and C are chosen to cause a delay longer than the expected transition times being sensed.

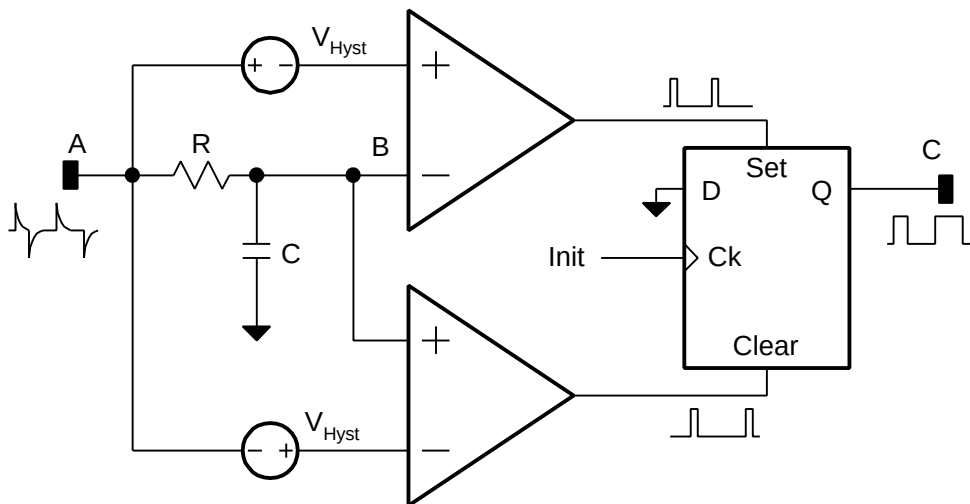


Figure 22: A simple test receiver implementation possibility for the concept in Figure 21.

NOTE 1 – Typical values of R and C might be 10 Kohms and 5 picofarads which could be integrated into an IC.

NOTE 2 – The input waveform at point A may be high-pass filtered (as shown) by AC coupling, or it could be a normal DC coupled digital waveform (with an unknown offset). In either case, the edges are used to reconstruct the original digital waveform.

NOTE 3 – The D-type flip-flop element can be initialized to zero by a clock signal “Init” to establish a known initial state at the start of testing.

Figure 23 shows an AC coupled differential signal channel from the drive side, done differentially, to the receive side which is single-ended for test purposes. (The mission receiver has been omitted for clarity.)

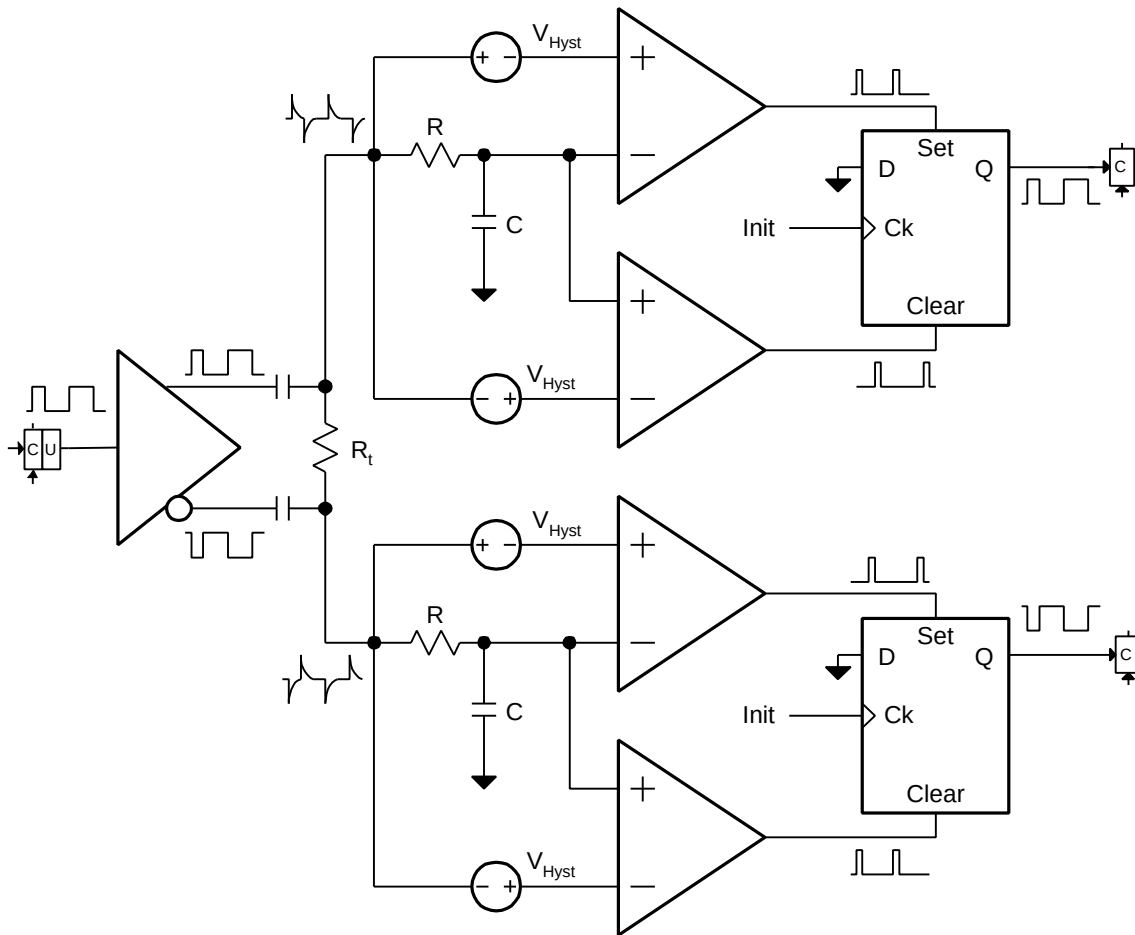


Figure 23: Differential driver, AC coupling, and receiver testability structure.

4.7 Test Receiver Support for the (DC) EXTEST Instruction

So far the test receiver behavior for AC EXTEST has been described. However it is important to support the standard (DC) EXTEST instruction. This amounts to “turning off” the edge integrating capability of the test receiver and having it respond to levels. This is further complicated by the problem that there may be common mode offsets added to the signals. This necessitates generating a reference voltage that can be used for single-ended comparison.

One way to do this is by “ V_{Com} recovery”, where the common mode voltage of the differential pair is derived from the signals on the pair as shown in Figure 24.

NOTE – If the differential receiver is DC coupled to a differential driver, then the differential driver will determine V_{Com} . If the receiver is AC coupled to a differential driver, then the receiver’s internal bias generator (or externally provided bias network) will determine the value of V_{Com} . In either case, the recovered voltage will suffice as a comparison reference.

With a derived V_{Com} it is possible to support EXTEST as shown in Figure 25.

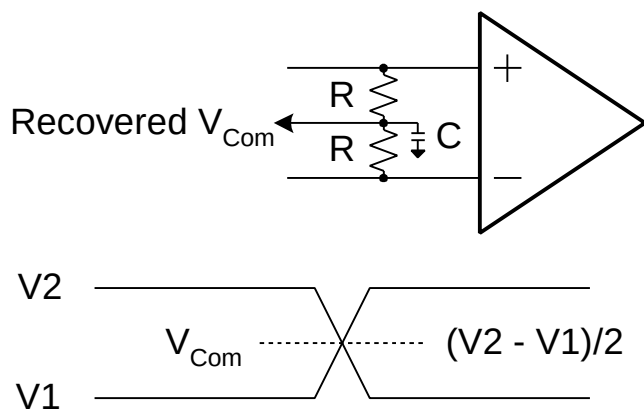


Figure 24: Technique to recover V_{Com} from a differential signal path.

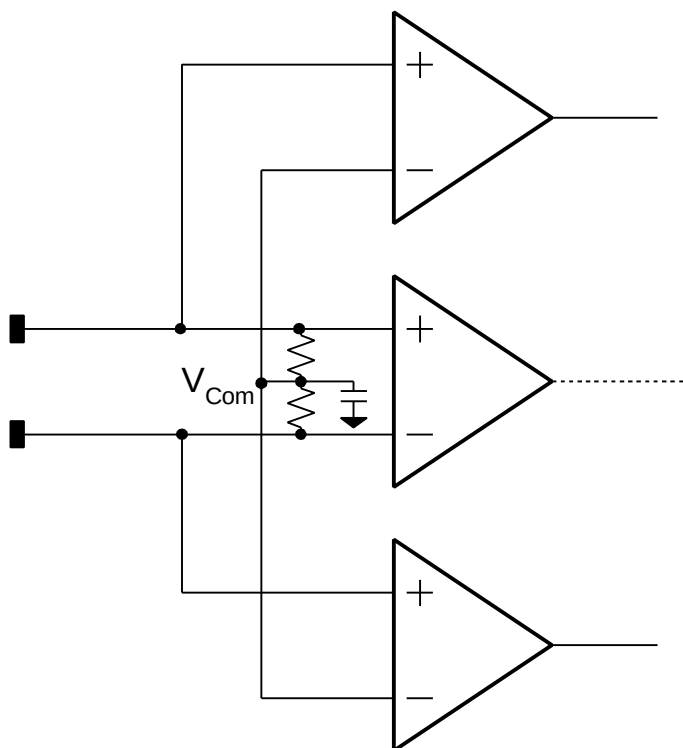


Figure 25: Simplified test receiver that supports (DC) EXTEST.

A criticism of the technique shown in Figure 25 is that the generated V_{Com} value is potentially a function of a defect in either leg. For example, if one receiver input pin is open, then the value of V_{Com} will track the other leg, with low-pass filtering. While this is not ideal, it will not result in a test that overlooks a defect (i.e., a false pass). One or both test receivers will perceive the defect.

4.8 A General Test Receiver for DC and AC EXTEST Instructions

A test receiver that supports both the AC and (DC) EXTEST instructions is required. This could be accomplished simply by taking the two structures already shown and selecting between them with multiplexers. However it is possible to merge their behaviors into a more efficient structure as shown in Figure 26. In this structure a silicon switch (with series impedance R_s which is perhaps 1/10 of R) is closed to perform V_{Com} recovery needed for DC EXTEST support, while it is opened to allow transition detection needed for AC EXTEST support.

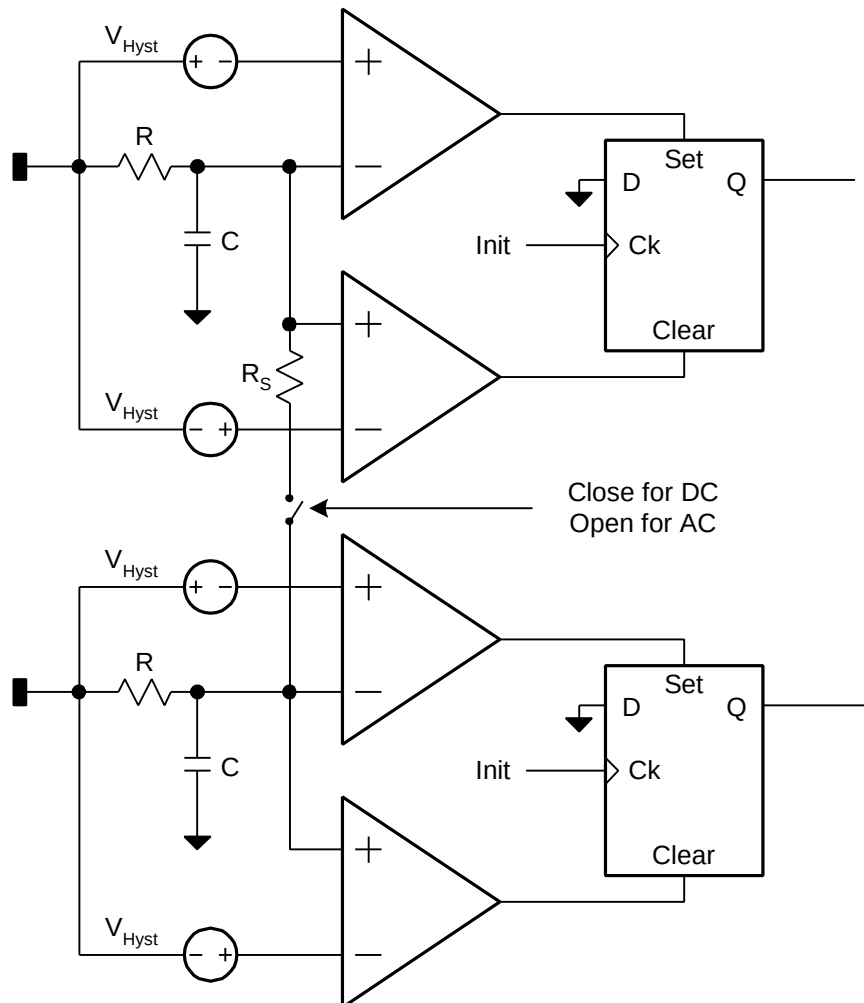


Figure 26: A test receiver structure that supports both AC and (DC) EXTEST.