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Draft Standard for Boundary-Scan Testing of Advanced Digital Networks

Prepared by the Advanced I/O Working Group
of the Test Technology Standards Committee
of the IEEE Computer Society

Abstract: This standard augments IEEE Std 1149.1 to improve the ability for testing differential and/or AC coupled interconnections between Integrated Circuits on boards and systems.

Keywords: AC Coupled Signals, Boundary-Scan, Differential Signaling, Interconnect Testing

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Introduction

(This introduction is not part of this standard.)

The development of this standard was begun May 21, 2001 by an ad-hoc industry Working Group called by Agilent Technologies and Cisco Systems. This group formulated this draft standard, with the intention of handing it over to the IEEE for formal standardization when the underlying technology became understood.

The group adopted as its mission:

> To define, document and promote a means for designing ICs that support robust Boundary-Scan testing of boards where signal pathways make use of differential signaling and/or AC coupled technologies. This technology utilizes and is compatible with the existing IEEE 1149.1 standard. The goal is to upgrade the capabilities of IEEE Std 1149.1-2001 to maintain the rapid and accurate detection and diagnosis of interconnection defects in boards and systems despite the fault masking effects of differential signaling and the DC blocking effects of AC coupled signaling.

The group first referred to itself as the "AC EXTEST" working group, but since expanded its charter to consider topics now called "Advanced I/O". At the time of issue of this draft the members ("*" indicates voting member) of the Working Group were:

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1 Overview

1.1 Scope

This standard defines extensions to IEEE Std 1149.1-2001 to standardize the Boundary-Scan structures and methods required to ensure simple, robust, and minimally intrusive Boundary-Scan testing of advanced digital networks. Such networks are not adequately addressed by existing standards, especially for those networks that are AC coupled, differential, or both. Testing enabled by this standard will operate in parallel with IEEE Std 1149.1 testing of conventional digital networks and in conjunction with IEEE Std 1149.4 testing of conventional analog networks. This standard also specifies software and BSDL extensions to IEEE Std 1149.1-2001, which are required to support new I/O test structures.

1.2 Organization of the Standard

Clause 1, "Overview" (informative) provides an overview and context for this standard.

Clause 2, "References" (informative) provides references necessary to understand this standard.

Clause 3, "Definitions and Acronyms" (informative) defines terminology and acronyms used in this standard.

Clause 4, "Technology" (informative) outlines the technologies addressed and utilized by this standard.

Clause 5, "TAP Instructions" (normative) provides rules for TAP instructions used for testing.

Clause 6, "Pin Implementation Specifications" (normative) provides rules for I/O pin implementation.

Clause 7, "Conformance and Documentation Requirements" (normative) provides rules for conformance and documentation of devices designed to this standard.

Clause 8, "Applications and Tools" (informative) shows how this standard is used in typical testing applications, and how devices conforming to this standard can be verified before manufacture, and tested in production.

1.3 Context

Figure 1 shows a printed circuit board containing many types of devices. Of these, some could be compliant with IEEE Std 1149.1 for the support of testing activities. These devices contain Boundary-Scan testability circuitry which allows them to participate in manufacturing tests that detect and diagnose faults such as open solder joints, shorts and missing devices.

The additional testability elements added by this standard to these same ICs allow this interconnect testing to be conducted on differential signal pathways and/or where AC coupling (which blocks normal DC test signals) has been used on signal paths between ICs.

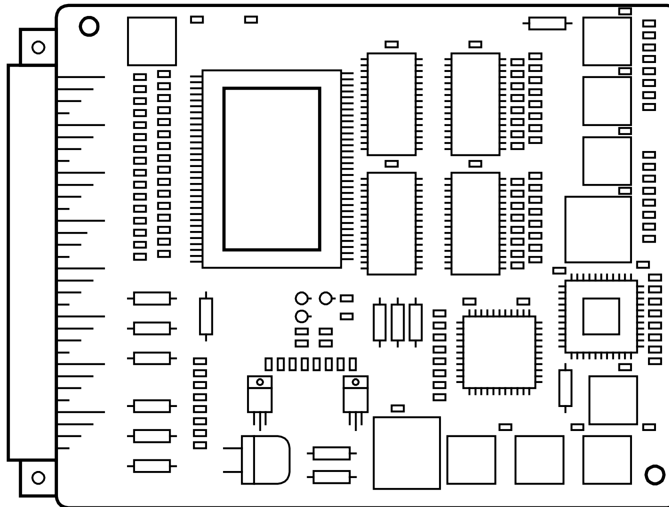
1.4 Objectives

The objective of this standard is to provide design guidance for testability circuitry added to an IC in addition to testability provisions specified by IEEE Std 1149.1, such that when such an IC contains differential signaling and/or is AC coupled with other ICs compliant to this standard, board and system level tests can be readily and accurately conducted.

1 Devices that adhere to this standard that are used in differential and/or AC coupled signaling
2 environments will realize significant savings in testing costs for boards and systems. Tools that
3 are cognizant of the capabilities provided by this standard will be able to prepare, run and
4 interpret these tests in a highly automated fashion, with high diagnostic resolution.

5 This standard allows devices created by multiple vendors to operate together during testing
6 despite the differing characteristics and parameters of the IC processes used to fabricate the
7 devices.

8 This standard also provides design guidance to board and system designers that will enhance the
9 performance of the testability features of their products. This in turn will reduce system and
10 production costs.



11 **Figure 1: A printed circuit board containing a variety of components interconnected by printed**
12 **wiring. Some ICs contain IEEE 1149.1 features that support Boundary-Scan interconnect testing.**

2 References

This document shall be used in conjunction with the following standards. When the following standards are superseded by an approved revision, the revision shall apply.

IEEE Std 100-1996, IEEE Standard Dictionary of Electrical and Electronic Terms.

IEEE Std 1149.4-1999 IEEE Standard for a Mixed Signal Test Bus.

IEEE Std 1149.1-2001, IEEE Standard Test Access Port and Boundary-Scan Architecture.

3 Definitions and Acronyms

In the following definitions, defined terms appear in **bold font**.

3.1 Definitions

Defined terms appear in **bold type**.

AC Coupling: The use of series capacitance in a **signal path**. This coupling will block DC voltages on the drive side of the path from appearing on the receive side. Only the AC component of the driven signal will pass through the coupling, with the effect of high-pass filtering imposed on the original signal. *Contrast with* **DC coupling**.

NOTE – AC coupling may also be accomplished with transformers which, as with capacitive coupling form a **high-pass filtered** transmission structure. While the principles used in this standard can be applied to transformer coupling, this coupling technology is less often used and is thus ignored to simplify discussion.

AC Pins: Device signal pins that are the target of the rules of this standard. AC pins may be **AC coupled** and/or **DC coupled** and may also be differential. *Contrast with* **DC Pins**.

AC Test mode: A **test mode** that enables Boundary-Scan testing between **AC pins** that are **AC Coupled** or **DC Coupled**. AC testing of DC coupled pins may enable testing that cannot be supported in **DC Test Mode** due to level incompatibilities. *Contrast with* **DC Test mode**.

AC Test Signal: A signal generated by the **AC test mode** that is used to modulate static test data into a time varying signal that can pass through **AC coupling**. A test receiver and detector is used to recover the static test data value from within the time varying signal.

Bias: A high impedance (typically >1000 ohms) voltage source often used on the input of a receiver to cause it to output a deterministic state in the absence of an input signal, and/or to select the **common mode voltage** seen by a **differential receiver** in **AC coupled** signal paths.

Bias network: A network of impedances, usually higher-valued than **termination** impedances and usually located in or near the receiver, used to establish a **common mode** or **reference voltage**.

Boundary-Scan testing: Testing of interconnections between IC pins as supported by IEEE Std 1149.1 and this standard. This testing technology looks for manufacturing defects along **signal paths**, which include open solder joints, broken bond wires, shorted signal traces, damaged drivers and receivers, etc. Tests are performed on many paths in parallel.

Channel: A **signal path** or set of signal paths that transmits a single data stream from a source to a destination. *See* **differential signaling** *and* **single-ended signaling**.

Characteristic Impedance: the ratio of the complex voltage and complex current of a signal traveling forward on a conductive path. A signal path is often **terminated** with an impedance that matches the characteristic impedance

of the path. This makes the path appear to be infinitely long and prevents signal degradation due to reflections that occur at unterminated ends of the path. *See* **termination**.

Common mode noise: A noise signal added equally to both **signal paths** in a differential signal **channel**. Common node noise will affect or completely disrupt a **single-ended** measurement of a signal on one leg of a **differential receiver**, yet this receiver will accurately recover the signal within the noise.

Common mode range: The range of common mode voltage that a differential receiver is capable receiving while maintaining reliable signal recovery. A differential signal with common mode voltage within this range will be received correctly. Outside this range the receiver may fail to recover the data signal.

Common mode voltage: The offset from ground of the mean of the maximum and minimum voltages that appear on a pair of differential signals. A **differential driver** will, by its operational characteristics, define a common mode voltage. A **differential receiver** will properly receive data over a range of common mode voltages, but will likely have an optimal common mode voltage where its performance is best. When the optimal common mode voltage of a receiver is significantly different than that of it associated driver, **AC coupling** with appropriate **bias** can be used to match the two components of a differential **signal path**.

Comparator: An amplifier with two inputs labeled positive and negative, typically with very high input impedance. The amplifier usually has very high gain and produces an output signal that is the amplified difference of the positive and negative input signals. For all but the smallest differences, the output will be V_{max} or V_{min}, which are the most positive and most negative voltages the amplifier can produce on its output. A comparator can be used as a differential receiver. A comparator can be used to determine if an input signal is logically above or below a reference voltage.

Current signaling: A signal encoded by the amplitude and direction of current flow. In a differential pair, a current signal is positive when current flows from positive to negative legs, and negative in the reverse direction. The voltage that may appear on these same legs does not carry information. *Contrast with* **voltage signaling**.

DC Coupling: The use of simple wires or small series resistances in a signal path. *Contrast with* **AC coupling**.

DC Pins: Device signal pins that are equipped solely with test resources defined by IEEE Std 1149.1. DC pins that are **AC coupled** are not testable as a **signal path**, but may be testable as logically independent pins if there are enough test resources on each pin. *Contrast with* **AC Pins**.

DC Test mode: A **test mode** that enables traditional **Boundary-Scan testing** between **DC pins** that are **DC Coupled**. *Contrast with* **AC Test mode**.

Defect: A defect is an unacceptable deviation from a norm; for example, an open solder joint. Because it is unacceptable, some remedial action is required and we need a way to find defects. *See* **manufacturing process defect** and **fault**.

Derived voltage reference: a voltage reference derived from: 1) other references, such as a resistive divider between power and ground, or 2) a resistive divider between two differential signals that recovers the common mode voltage of the signals.

Differential driver: A driver that accepts a single data stream and drives it onto two independent signal paths where one signal is the inverse of the other. The two signals are centered at the common mode voltage.

Differential receiver: A receiver that recovers a single data stream encoded differentially on two signal paths. It effectively subtracts the signal on its negative leg from that on its positive leg. This eliminates **common mode noise** appearing on both legs.

Differential signaling: The use of two independent signal paths in a channel to carry a single data signal, where one path carries an inverted copy of the signal that appears on the other path. The original data signal can be reconstructed by taking the difference of the two signals and there is no reliance on a reference voltage for determining this signal. This has the property of eliminating **common mode noise** in the transmitted signal. *Contrast with* **single-ended signaling**.

Encoding protocol: A stream of data bits may be encoded into a new (typically longer) data stream that has characteristics favorable for its transmission on a **channel**. The encoded stream may have added redundancy to support error correction. The encoded stream may have extra bits added to deliberately increase the number of transitions that appear in the stream, effectively raising its apparent **frequency** and facilitating data transmission that encodes clocking information into the stream.

Fault: A fault is a physical manifestation of a **defect**. For example, an open solder joint (a defect) on the input to an IC may cause one or more of its outputs to produce incorrect data (a fault). In many cases, a fault and its causal defect are not co-located.

Frequency: The maximum number (f) of transition pairs that occur on a signal path expressed in Hertz (cycles per second). With respect to **AC Coupling**, a frequency is *high* when the period ($1/f$) is small compared to the **time constant** of the coupling. A frequency is *low* when the period is large compared to the time constant of the coupling. The frequency appearing on a signal path may vary greatly over time as a function of the data being transmitted and the data **encoding protocol**.

Float: The input to a receiver that is connected to an undriven signal, or a high impedance connection to a receiver input, is said to *float*.

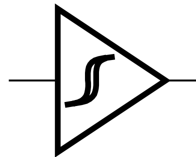
High pass filter: An electrical network that passes higher frequencies and attenuates lower frequencies. DC current is blocked.

HP_Mult: High-Pass Multiplier, a multiplier used to derive the minimum high-pass coupling time constant. (See sections 6.2.3.1 and 6.2.3.3.)

HPLP_Ratio: High-Pass-Low-Pass Ratio, a multiplier used to derive the minimum ratio of high-pass coupling time constant (**HP_Mult**) to low-pass filter time constant (**LP_Mult**). (See sections 6.2.3.1 and 6.2.3.3.)

Hysteresis: From magnetics: lagging in the values of resulting magnetization in a magnetic material (such as iron) subjected to a changing magnetizing force. In this document, hysteresis refers to the memory of an input state to an amplifier or buffer after that state is removed but before a different input state is applied. Typically there is a hysteresis threshold that defines the difference between “no input” and “input.” As applied to electronics, a digital output circuit such as a comparator where the output switches to one output state when the input is above one level and switches to the opposite output state when the input is below a lower level, and the output does not switch at any intermediate level. Example: a buffer produces a high output when a voltage above 0.5 volts is applied, produces a low output when a voltage below 0.3 volts is applied, and does not change its output for voltages between 0.3 and 0.5 volts.

Hysteresis symbol in a buffer symbol:



Hysteretic: Adjective form of **hysteresis,** as in “hysteretic amplifier.”

Interconnect test: An IEEE Std 1149.1 Boundary-Scan test designed to detect and diagnose defects in the interconnection wiring between ICs. This standard extends the concept to include the testing of channels, where single-ended and differential signaling, and DC or AC coupling may exist.

Load termination: A **termination** placed at the far end (away from the driver) of a **signal path** used to match the **characteristic impedance** of the path. *Contrast with* **source termination**.

Low pass filter: An electrical network that passes lower frequencies, including DC levels, and attenuates higher frequencies.

LP_Mult: Low-Pass Multiplier, a multiplier used to derive the minimum low-pass filter time constant. (See sections 6.2.3.1 and 6.2.3.3.)

Manufacturing process defect: A **defect** that is a byproduct of the board manufacturing process. These include missing devices (ICs, resistors, capacitors, etc.), improperly mounted devices (e.g., rotated 180 degrees), open solder joints, shorted solder joints, misaligned devices, incorrect and dead devices.

Mission logic: The circuitry inside an IC that performs its primary design function. *Contrast with* **test logic**.

Mission mode: A device performing its primary design function. *Contrast with* **test mode**.

Negative leg: The signal path of a differential signal pair that has the opposite polarity as the original data signal.

Null: The input state where the two inputs to a differential receiver which are supposed to be different (complementary) are instead receiving the same value.

Offset voltage: A constant DC voltage added to an AC signal.

1 **Operational modes:** A device may operate in one of two modes, see **mission mode** and **test**
2 **mode**.

3 **Positive leg:** The signal path of a differential signal pair that has the same polarity as
4 the original data signal.

5 **Reference voltage:** A low impedance voltage source typically used to define a threshold for
6 comparing signals. The low impedance characteristic means it is resistant
7 to conducting noise signals.

8 **Referenced termination:** A termination for a differential channel where the two legs are both
9 terminated to a reference voltage. This reference has a low enough
10 impedance such that the two legs are independent.

11 **Self-referenced comparison:** The comparison of a signal with a delayed, averaged version of the
12 same signal, used to detect signal transitions. This process does not need
13 a static reference voltage to find a transition in a signal.

14 **Signal Path:** An electrical pathway formed by a simple conductor, or a terminated
15 pathway containing a series resistance, or an AC coupled pathway
16 containing a series capacitance, that transmits a signal from a driver to a
17 receiver.

18 **Signal reflection:** A signal wavefront traveling across a discontinuity in the **characteristic**
19 **impedance** of the **signal path** may have a fraction of its energy reflected
20 in the opposite direction on the path. The reflection may be of the same
21 or opposite polarity and will add into the waveforms appearing on the
22 path, impacting their shape. *See also* **transmission line**.

23 **Single-ended signaling:** The use of a single signal path in a channel to carry a data signal. The
24 signal is referenced to a static reference voltage. *Contrast with*
25 **differential signaling**.

26 **Slew rate**: Rate of change in either direction of voltage in a specified time,
27 measured in units of volts per second.

28 **Source termination**: A **termination** placed near the source driver of a signal, to satisfy DC
29 current requirements of a driver and/or to match the **characteristic**
30 **impedance** of a **transmission line** structure to reduce **signal reflections**.
31 *Contrast with* **load termination**.

32 **Termination**: An impedance usually near the end of a signal path used to satisfy the
33 electrical matching requirements of the **characteristic impedance** of the
34 **signal path** and reduce **signal reflections**. The impedance is typically
35 low, often 100 ohms or less. *See also* **characteristic impedance**,
36 **referenced termination, source termination, load termination** *and*
37 **unreferenced termination**.

38 **Test logic:** Testability logic defined by this standard and the IEEE Std 1149.1 and
39 IEEE Std 1149.4 standards. *Contrast with* **mission logic**.

40 **Test mode:** A device or pin of a device that, in response to the EXTEST or an AC
41 testing instruction, is now driving and/or receiving test data as controlled
42 by the test logic of the IC. It has been disconnected from the internal
43 mission logic of the IC. *Contrast with* **mission mode**.

Test receiver: A circuit that examines an incoming signal, which can operate in **AC test mode** and **DC test mode**. Its purpose is to extract test data from a signal that may have been altered by DC level shifting or AC coupling decay.

Time constant: Typically the product of resistance and capacitance of an RC network (e.g., a high pass filter) measured in seconds. One time constant is the time for a capacitor to discharge 63% of its voltage through a resistor. In AC coupled systems, the termination resistance combined with the coupling capacitor forms a **high pass filter**.

NOTE – In discussions comparing time periods to time constants, a period is *significantly* longer (shorter) than a time constant if it is five (one-fifth) times the time constant value. For example as shown in Figure 2 using the five-time-constant rule, a signal will decay to 0.7% of its original value. The one-fifth-time-constant rule means that 81.9% of a signal still remains.

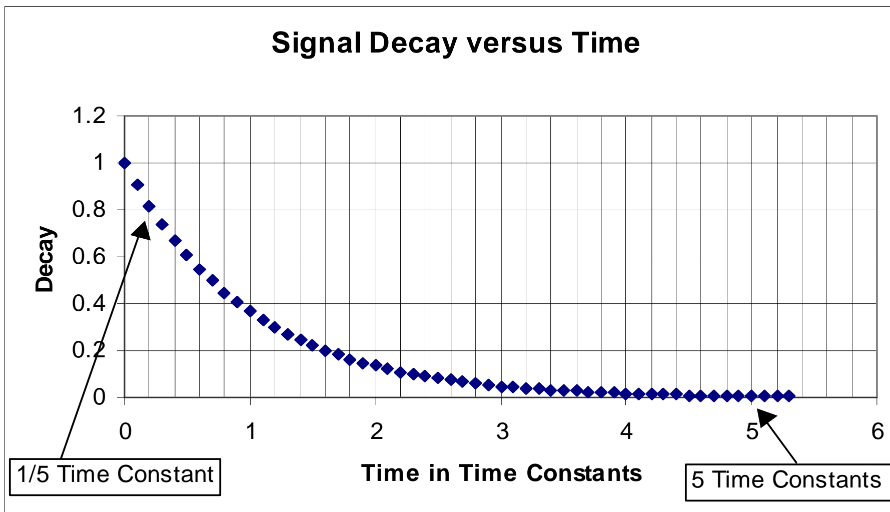


Figure 2: Signal decay versus time in units of time constants.

Transition: A voltage transition occurs when a signal traverses a specified voltage range in a specified time in either direction. *See* **slew rate.**

Transmission line: A **signal path** with a specific construction that produces a uniform, known **characteristic impedance** along its length. This minimizes degradation of a signal passing along this path that can result from impedance variations.

Unreferenced termination: A termination for a differential channel where a termination impedance is connected between the two legs with no connection to a reference voltage.

Voltage signaling: Signals are encoded by the voltage appearing on a wire compared to a reference voltage (single-ended) or the voltage appearing on a pair of wires (differential). *Contrast with* **current signaling**.

3.2 Acronyms

CML: Current mode logic

HP_Mult High-Pass Multiplier

HPLP_Ratio High-Pass-Low_Pass Ratio

1 **HSTL:** High-Speed Transceiver Logic

2 **LP_Mult:** Low-Pass Multiplier

3 **LVDS:** Low Voltage Differential Signaling

4 **LVPECL:** Low voltage PECL (Pseudo Emitter Coupled Logic)

5 **PECL:** Pseudo Emitter Coupled Logic

6 **TAP:** Test Access Port (from IEEE Std 1149.1).

4 Technology

The presence of coupling capacitors on chip interconnects, whether they are discreet devices mounted on a PC board or integrated inside an IC, prevents DC values from being driven between a driver and receiver. An AC Boundary-Scan methodology must therefore use a time-varying signal to pass through the AC coupling when in AC Test mode.

Differential signaling is often used to increase signaling speeds and noise immunity, compared to single-ended coupling. Differential signaling, combined with termination schemes, can have significant defect masking properties that reduce test effectiveness. (See section 4.3.)

4.1 Signal Pin Types

It is expected that a chip possessing pins requiring AC coupling may also possess "normal" (i.e, DC coupled) pins as well. These DC pins would supply data and/or control to/from portions of the chip that do not require AC coupling. For test purposes, it is necessary that all these pins be tested simultaneously with an EXTEST-like capability because that is how shorts (unwanted connectivity) between these pins are reliably detected and diagnosed. It is desirable for higher test throughput to test all pins simultaneously with an EXTEST-like capability as well. This document will refer to DC and AC pins henceforth. DC pins are those that IEEE Std 1149.1 currently governs for testing. AC pins were not considered during the development of IEEE Std 1149.1, so no guidance appears in that standard on how to test them.

AC pins are a principle target of this standard. IC designers implementing this standard are expected to identify such pins and add new test capabilities for them.

4.2 Signal Coupling and Coupling Combinations

This section reviews a range of coupling options.

4.2.1 Single-ended DC

A basic, single-ended connection scheme is shown in Figure 3, along with the Boundary-Scan control and observation capability specified by IEEE Std 1149.1. This type of coupling has been quite common and is very testable using Boundary-Scan.

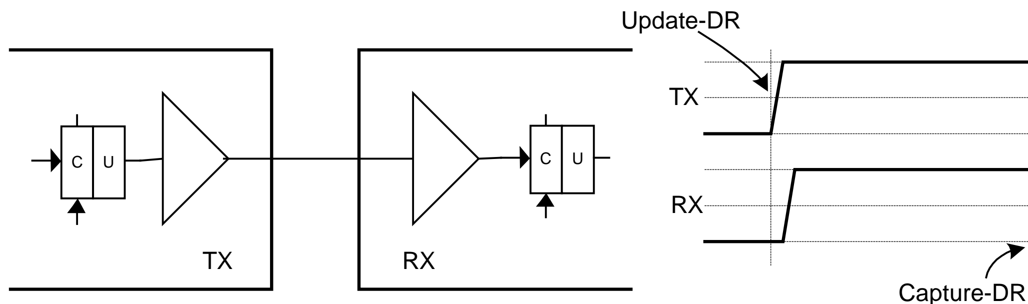


Figure 3: Basic single-ended signaling with Boundary-Scan control and observation.

It is important to note that in a standard Boundary-Scan test, the time between launching a signal from a driver (at the falling edge of TCK in the Update-DR or Update-IR TAP controller state) and capturing that signal (at the rising edge of TCK in the Capture-DR TAP controller state) is no less than 2.5 TCK cycles. Further, the time between successive launches on a driver is governed not only by the TCK rate, but by the amount of serial data shifting needed to load the next pattern

data in the accumulated Boundary Registers of the Boundary-Scan chain. Thus the effective test data rate of a driver could be thousands of times lower than the TCK rate. For DC coupled interconnect this time is of no concern. For AC coupled interconnect, the signal may easily decay partially or completely before it can be captured. If only partial decay occurs before capture, that decay will very likely be completed before the next edge is produced by the driver.

4.2.2 Single-ended AC

Figure 4 shows an AC coupled single-ended connection. (The termination resistor and voltage source shown may not be necessary thus would be omitted.) While the devices may have been designed for DC coupling and actually contain Boundary-Scan resources, the AC coupling will block their operation. This interconnection configuration could only be tested at very high test clock (TCK) frequencies and even then the results may be unreliable. TCK frequencies are likely to be significantly lower than the normal operating frequency of the channel being tested. Thus the data seen by the receiver may decay before it can be captured.

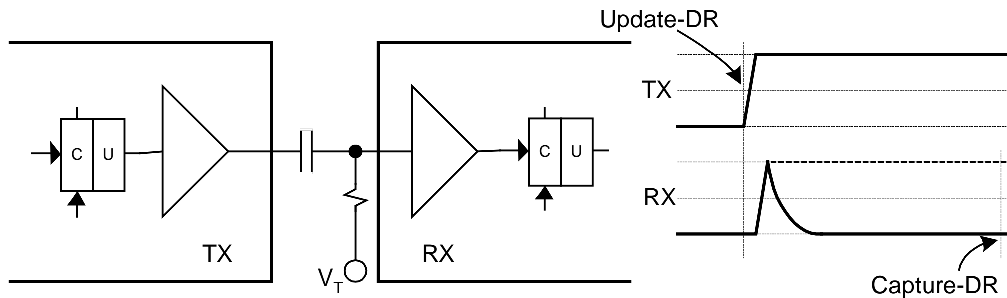


Figure 4: Basic single-ended signaling with AC coupling.

In general, AC coupling can distort a signal transmitted across a channel depending on its frequency. For example, Figure 5 shows a channel transmitting a high and low frequency waveform across an AC channel and observed at the input of the receiver. The high frequency signal is relatively unaffected by the coupling. The low frequency signal is severely impacted. First, it decays to V_T after a few time constants. Second, its amplitude is double the input amplitude. A key item to note is that the transitions in the original signal are preserved, although their start and end points are offset compared to where they were in the high frequency case.

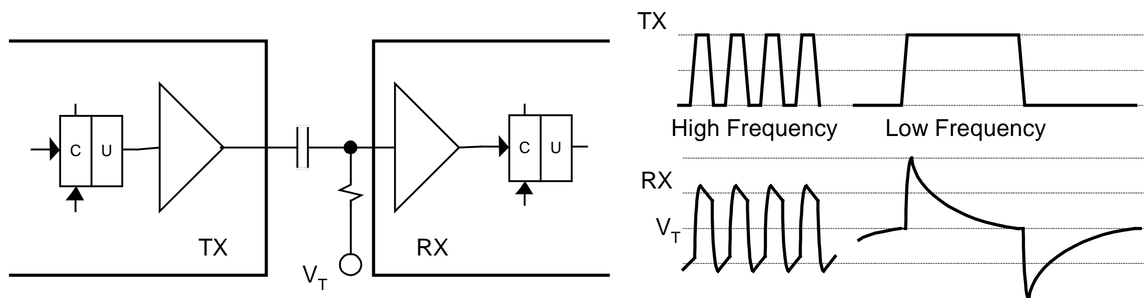


Figure 5: High and low frequency response of an AC coupled channel.

4.2.3 Differential DC

Figure 6 shows a basic differential DC coupled signal path. The termination resistor may exist for impedance matching and/or source termination of the driver. The placement of Boundary-Scan resources is optional per IEEE Std 1149.1 in that they can be omitted altogether. The 1149.1 standard allows a designer to designate the differential signal path as “analog”. Then the digital-to-analog and analog-to-digital interfaces (optionally) can be provided with Boundary-Scan

resources as shown in Figure 6. When this option is taken, it is then possible to test the “analog” signal path with Boundary-Scan algorithms. In this case the signal path is viewed by the test logic as if it were single-ended, leading to diagnostic ambiguity.

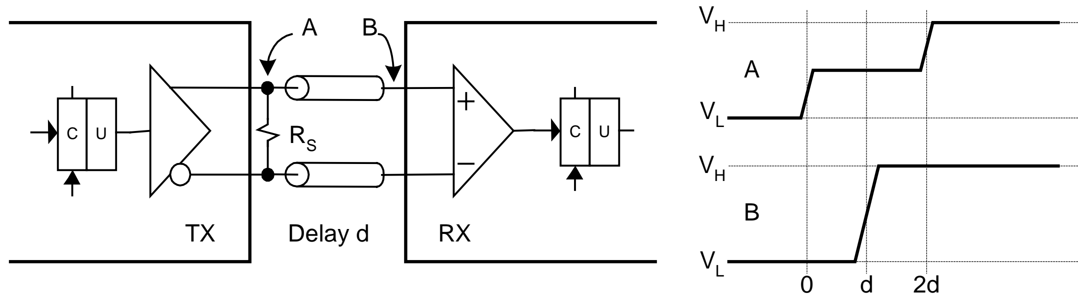


Figure 6: Basic differential signaling with DC coupling and source loading.

The driver in Figure 6 could be producing a voltage signal and the resistor is used to match the signal line impedance. Alternatively, the driver could be producing a current signal, where the direction of flow represents data, and the resistor is needed not only to match signal line impedance, but also to provide a DC current path to satisfy the driver’s requirements. This is called a source termination.

The driver in Figure 6 is looking into a termination R_S and transmission lines with characteristic impedance R_S as well. This forms a voltage divider which sends ½ the signal into the transmission lines. When the signal wavefront reaches the receiver (after delay d) its high impedance does not match the characteristic impedance which reflects the signal back down the lines to the receiver. This signal (1/2 the driver voltage) adds to the signal received so that the receiver perceives a full voltage swing. After the second transmission line delay d, the reflected signal reaches the driver and brings the voltage seen there to the full level. Thus a clean transition is seen at the receiver, but the signal seen at the driver is a two-step staircase. Since there is an impedance match at the driver, no new reflections occur.

In the case where the impedance R_S is moved to the receiver, (to the right of the transmission lines) this is called load termination (and the resistor is renamed R_L) as shown in Figure 7. Now the driver is looking into the transmission lines with characteristic impedance R_L. The full waveform is transmitted (no divider is now present) and this edge propagates to the receiver. At the receiver the termination resistor matches the line impedance, and thus there is no reflection. The waveforms at both the driver and receiver are full transitions.

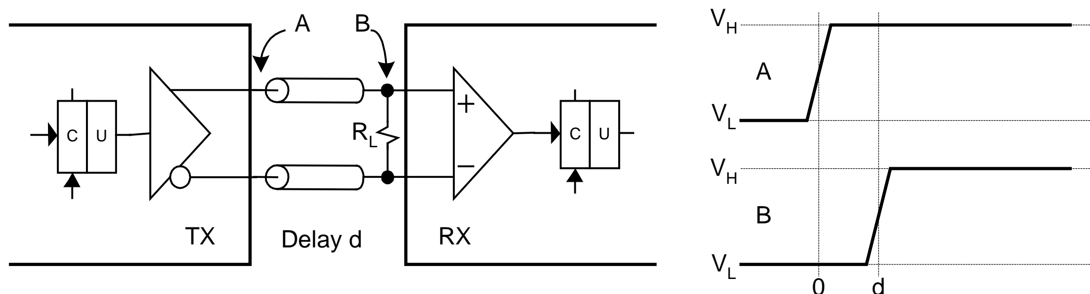


Figure 7: DC coupled driver and receiver with load termination.

Figure 8 shows a driver/receiver pair that has been both source and load terminated. In this case the voltage swing seen on both sides of the transmission line has been divided by two (note R_S

equals R_L). This type of termination assures that in the case of an imperfect impedance match, the resulting reflections can be attenuated at both ends of the line.

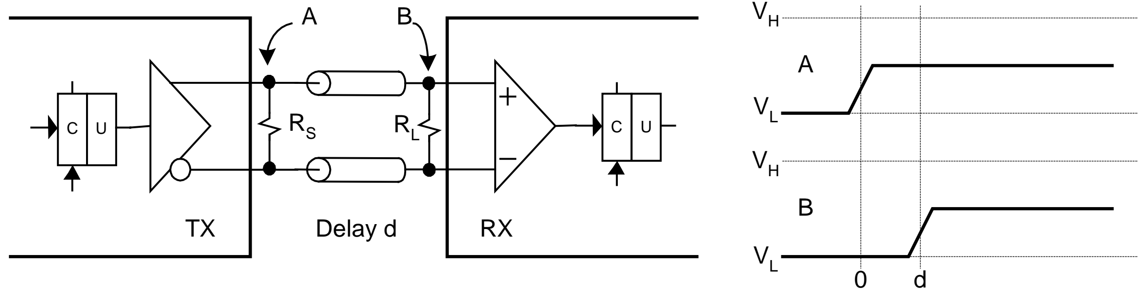


Figure 8: DC coupled driver and receiver with both source and load termination.

4.2.4 Differential AC

Figure 9 shows AC coupling of a voltage driver and receiver that could be completely incompatible for DC coupling because the voltage levels used by the driver are too far removed from the acceptable common mode range of the receiver. The termination network referenced to the common mode voltage source V_{Bias} (the optimal common mode point of the receiver) along with the DC blocking effect of the coupling capacitors, allows this configuration to work properly. This enforced compatibility is a common reason why board designers may use AC coupling.

NOTE 1 – The receiver waveforms in Figure 9 will decay to V_{Bias} if the driver frequency is low compared to the time constant of the coupling network. Since Boundary-Scan test data application rates can be low, the receiver may indeed see null levels due to signal decay.

NOTE 2 – It is assumed in Figure 9 that the distance between R_L and the receiver inputs is small, such that there are no significant transmission line effects beyond R_L.

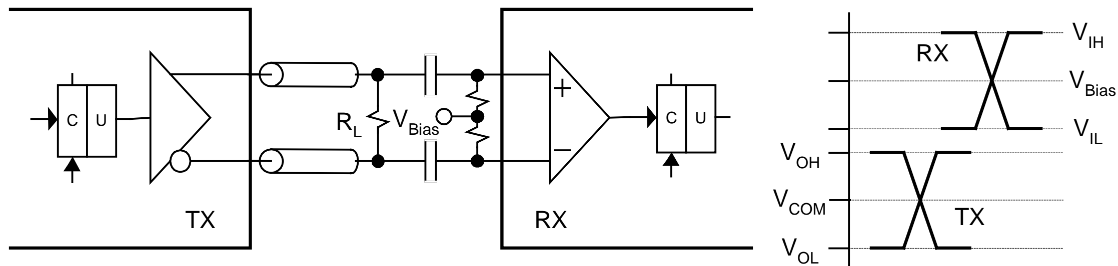
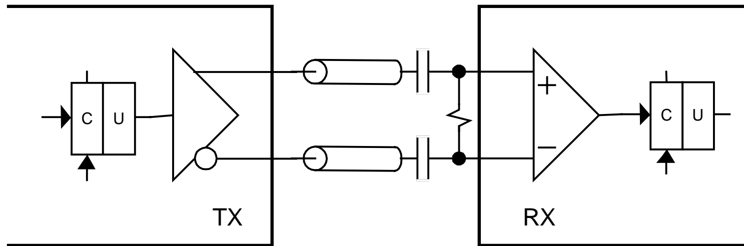


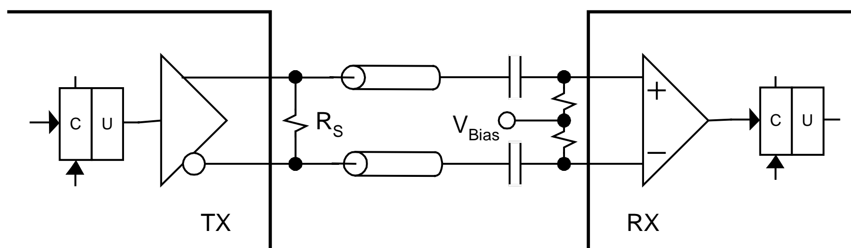
Figure 9: A basic differential AC signal path with load termination and receiver common mode generation using a bias network.

Figure 10 shows a basic differential AC signal path with an unreferenced termination. The termination is used for impedance matching. The driver is a voltage driver and thus does not need a source termination to provide a current path.



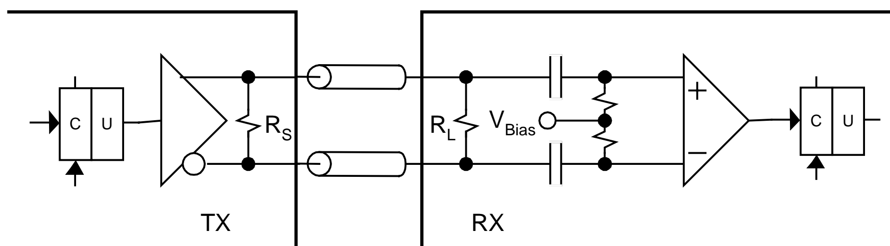
1 **Figure 10: A basic differential AC signal path with unreferenced termination.**

2 Figure 11 shows a basic differential AC signal path with a current driver and source termination,
3 and also a referenced bias generator to select the common mode voltage appropriate for the
4 receiver. The source termination may also serve as an impedance match for the line. The bias
5 network may use significantly larger resistors as long as the line distance from the capacitors to
6 the receiver is small. This will significantly increase the time constant of the coupling network.



7 **Figure 11: Basic differential AC signal path with source termination and bias provision.**

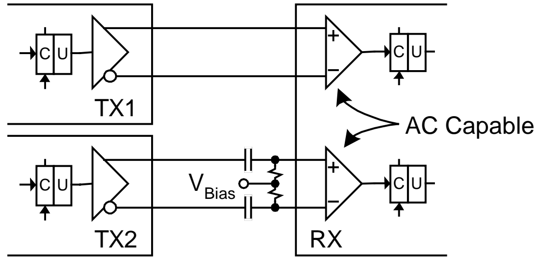
8 Finally, all the terminations, bias networks and even the coupling capacitors may ultimately be
9 integrated into the receiver IC. Externally, the signal path appears to be DC coupled but internally
10 it is still AC coupled, as shown in Figure 12. On-chip component defects will not need to be
11 tested during board test. Thus only the interconnect defects (typically solder) will be relevant.



12 **Figure 12: AC coupling, termination and bias generation internal to the ICs.**

13 4.2.5 Intention: When AC Capability Is DC Coupled

14 The standard for AC testing proposed herein is intended to be implemented on AC pins of an IC.
15 However, there is the possibility that a board designer may still choose to use DC coupling
16 between devices that are DC compatible. Thus a test developer could find a situation where AC
17 testing is needed to test a DC coupled signal path. This could occur when more than one AC-
18 capable interface exists on an IC and one is AC coupled while another is DC coupled. The test
19 developer would need to load an AC testing instruction into the device to test the AC coupled
20 interface. It is the intention of this standard that if DC coupling of AC-capable interface is
21 possible and gives acceptable mission performance, then the AC test performance will also be
22 acceptable.



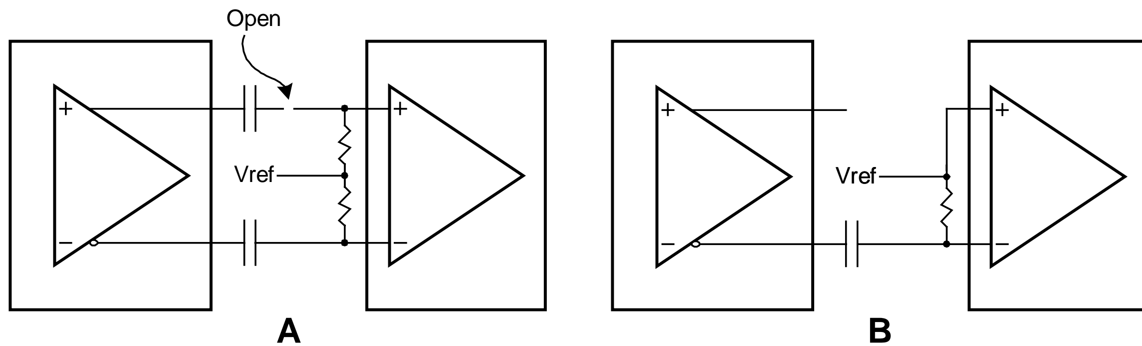
1 **Figure 13: An AC-capable receiver connected to an AC-capable driver and a conventional driver.**

2 For example, in Figure 13 a conventional IC (TX1, containing only EXTEST support) is DC
3 coupled to a receiver in RX. An AC-capable driver TX2 is also connected to the receiving IC. To
4 test all the signal paths simultaneously, the conventional device TX1 must be in EXTEST while
5 the other two use an AC testing instruction. See a summary of capture behaviors for various
6 coupling and testing scenarios given in section 4.10.

7 ### 4.3 The Effects of Defects

8 Defects are abnormalities in the structure of a board that occur during manufacturing that must be
9 found and corrected. This "manufacturing defect" model includes things like open solder joints,
10 shorts, missing components and dead devices. Not included in this model are performance-related
11 issues, for example, the failure of a device to operate at its highest specified frequency at –40
12 degrees. This recognizes the traditional role of IEEE 1149.1 as a test standard for manufacturing
13 defects.

14 The advent of AC coupling, especially in the differential signaling domain, threatens this role.
15 There is inherent redundancy in differential structures that can mask the presence of seemingly
16 obvious defects. An example is shown in Figure 14.



17 **Figure 14: An AC coupled differential path containing a defect (A) and an equivalent circuit (B).**

18 In this case, the positive leg of the circuit is eliminated by a defect, for example, an open solder
19 joint on the capacitor. Yet the receiver still receives the negative leg signal and compares it to the
20 V_{ref} voltage. The receiver will still produce the correct output, although its common mode noise
21 rejection capability is completely compromised. This might not be noticed until subsequent
22 functional or performance testing is encountered. There it may show up as an elevated bit error
23 rate that would not provide very much diagnostic information. This simple example illustrates
24 why it is important to monitor *both* legs of a differential pair, as covered in section 4.6.4.

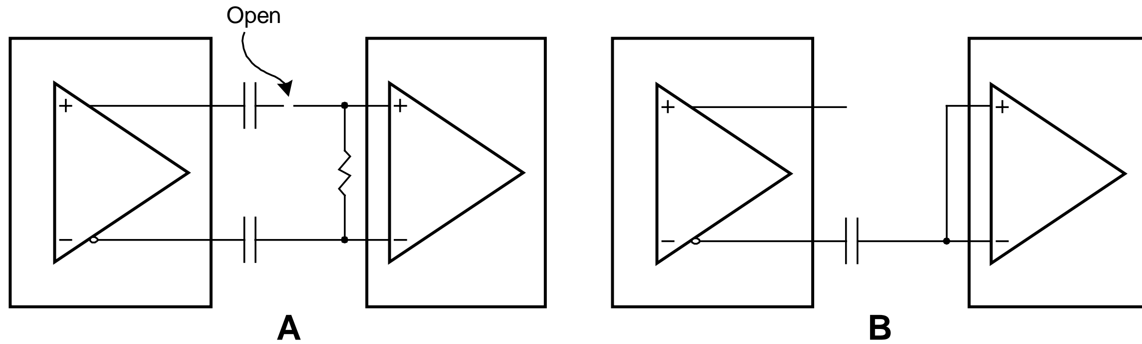


Figure 15: A null signal defect condition (A), where both legs see identical rather than complementary signals in the equivalent circuit (B).

Another defect scenario creates what is called the *null* signal condition, shown in Figure 15. As a result of unreferenced termination, the open defect allows the signal on the negative leg to appear on both legs of the receiver, in phase rather than 180 degrees out of phase.

One defect in particular may be troublesome to detect in AC coupled structures: the shorted capacitor. This defect restores DC coupling. This defect may go unnoticed particularly in differential signal paths, especially when the DC characteristics of the driver and receiver are similar. For this reason, it is important to support the standard EXTEST instruction, because it can be used to test for shorted capacitor defects. This can be done by supplying a stream of 0s and 1s to the driver side of the capacitor and showing that this stream does not show up on the receive side.

Finally, it is important to realize that defects that occur in high-speed circuits (where slew rates are often faster than signal path transmission times) the transmission lines may alter the circuit's faulty behavior as shown in Figure 16. Simulation of the circuit's behavior may be necessary to understand the effects of defects. It is important to consider transmission lines as components of the simulated model when slew rates are elevated.

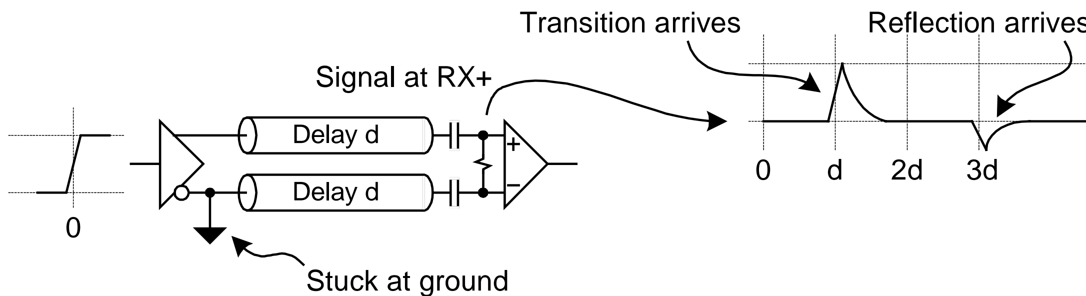


Figure 16: A defect may interact with transmission lines to produce unexpected effects.

4.4 Defects Targeted by this Standard

This standard (as well as IEEE Std 1149.1) provides test support for "manufacturing process defects" that are found on printed circuit boards coming out of the manufacturing process. These defects include missing devices (ICs, resistors, capacitors, etc.), improperly mounted devices (rotated 180 degrees), open solder joints, shorted solder joints, misaligned and dead devices. This standard focuses on those defects concentrated in AC coupled and/or differential channels. As seen in section 4.3, these defects may be difficult to detect, or may be effectively masked from detection. Figure 17 and Table 1 show a representative set of defects considered by this standard.

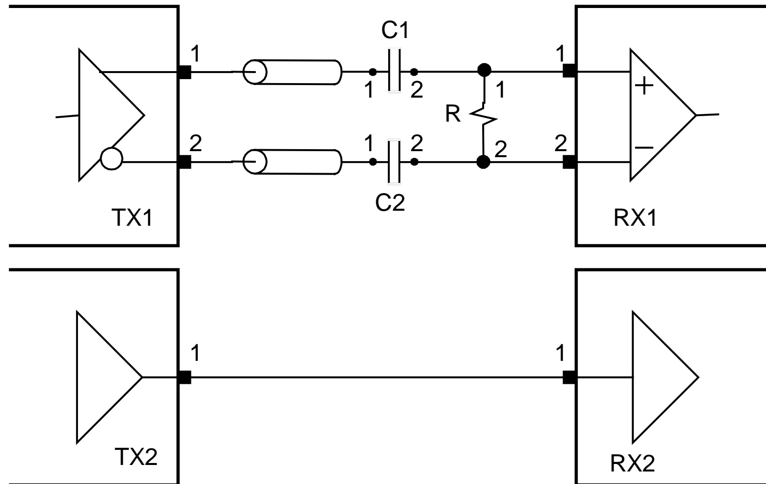


Figure 17: General AC coupled channel and nearby DC channel used to illustrate defects.

Table 1: Potential defects for the circuit in Figure 17.

Defect ID	Defect Site **(Note 1)**	Possible Defect Cause(s)	Comment
1	TX1 pin 1 open	Open solder joint, broken bond wire	Receiver sees null, possible reflection if termination is unreferenced (Note 2)
2	C1 pin 2 open	Open solder joint, missing capacitor	Receiver sees null if termination is unreferenced
3	RX1 pin 1 open	Open solder joint, broken bond wire	RX1 pin 1 floats
4	TX1 pin 1 short to VDD	Pin-to-pin short, solder splash	Possible reflection, receiver sees null if termination is unreferenced
5	TX1 pin 1 short to Ground	Pin-to-pin short, solder splash	Possible reflection, receiver sees null if termination is unreferenced
6	TX1 pins 1, 2 shorted together	Pin-to-pin short, solder splash	Receiver sees null if termination is unreferenced, no signal on either leg
7	C1 pins 1, 2 shorted together	Solder splash, internal short in C1	RX1 pin 1 is DC coupled, may pass EXTEST data
8	C1 pin 1 short to C2 pin 2	Pin-to-pin short, solder splash	Positive leg DC coupled to negative leg
9	RX1 pin 1 short to VDD	Pin-to-pin short, solder splash	Negative leg affected if termination is unreferenced
10	RX1 pin 1 short to Ground	Pin-to-pin short, solder splash	Negative leg affected if termination is unreferenced
11	RX1 pins 1, 2 shorted	Pin-to-pin short, solder splash	Receiver sees null, no signal on either leg
12	TX1 pin1 short to TX2 pin 1	Pin-to-pin short, solder splash	RX1 sees positive leg with distorted data
13	RX1 pin1 short to RX2 pin 1	Pin-to-pin short, solder splash	RX1 sees positive leg with TX2 data, negative leg affected if termination is unreferenced
14	R1, pin 1 open	Open solder joint, missing resistor	Receiver legs floating if not internally biased, affected leg(s) have impedance mismatch, much longer time constants

NOTE 1 – Defects that are equivalent by symmetry are omitted.

NOTE 2 – Referenced termination (to low impedance voltage sources) will isolate legs, while unreferenced termination will allow interactions between legs. This produces differences in faulty behavior.

4.5 Differential Termination and Testability

Extensive study of differential channels and the effects of defects within those channels has shown that the effects of defects are heavily influenced by the termination schemes used. There are three functions of terminations:

- to provide for proper DC paths needed for proper driver functioning, (usually source termination),
- to provide impedance matching of transmission lines, and
- in some AC coupled cases, to set common mode operating points for the receiver.

A given termination may provide one or more of these functions. The following subsections discuss termination options.

4.5.1 Unreferenced Termination

Source termination is usually needed for current signaling technologies, where the direction of current flow is used to encode binary data. A typical example is a Low Voltage Differential Signaling (LVDS) driver/receiver pair. Since all differential receivers operate by comparing voltages, a current signal is translated into a voltage signal for that comparison. Figure 18 shows an LVDS driver DC coupled to a voltage receiver, where R_S provides both source termination and impedance matching. The direction of current flow represents data.

NOTE – It is assumed that R_S is placed very close to the receiver so that any transmission line effects are only present between the driver and the resistor.

This form of termination is called unreferenced because there is a single resistor R_S rather than two resistors center tapped to a reference voltage (seen later in Figure 20). In effect, the receiver is referenced to the common mode voltage of the driver/resistor combination. This means the receiver's common mode range must be compatible with the driver's output.

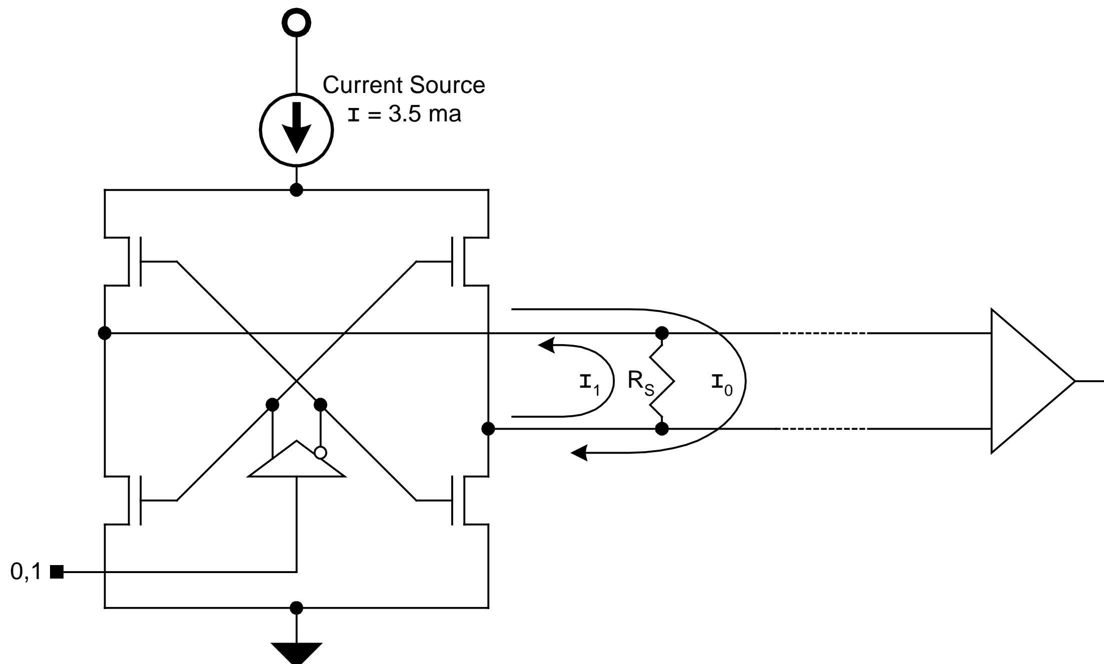


Figure 18: LVDS driver and receiver, DC coupled.

Figure 19 shows an unreferenced AC termination. Resistor R_S still provides source and line termination. Resistor R_L provides termination and a current path on the receive side, since the comparator input impedance is effectively infinity. Note R_L and C determine the time constant of this coupling.

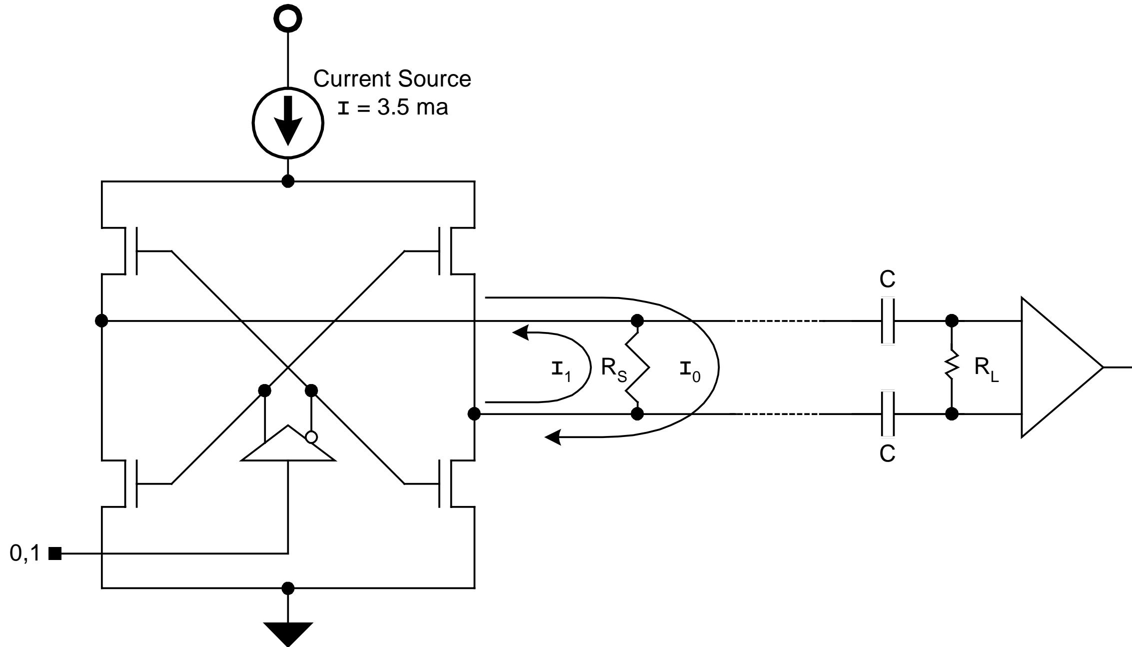


Figure 19: LVDS driver and receiver, AC coupled with unreferenced termination on the receive side.

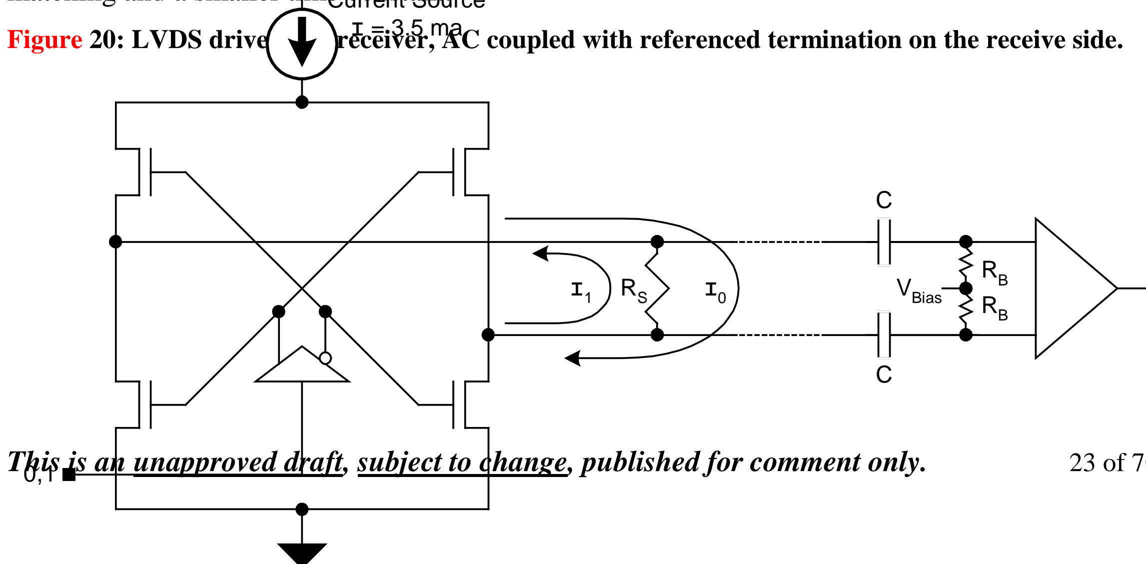
NOTE – The receiver in Figure 19 will have its own biasing circuitry built in to establish its common mode operating point.

If the time between signal transitions is long, the voltage across R_L will decay to zero volts, or a null input condition with results that may be undefined. Note that some defects can also cause this to occur, such as either capacitor C missing. A null input condition during testing is undesirable due to its non-determinism and the ways it can interact with defects (see 4.3) as seen by any Boundary-Scan register cell that monitors the mission receiver.

4.5.2 Referenced Termination

Figure 20 shows an AC coupled, referenced termination. This type of termination is used to set the common mode voltage of the receiver at its optimal value (here, V_T). Resistors R_B along with capacitance C determine the time constant of the coupling. The value of R_B may be larger, simply providing bias and a larger time constant, or may be smaller to provide both bias, load impedance matching and a smaller time constant.

Figure 20: LVDS driver and receiver, AC coupled with referenced termination on the receive side.



In the referenced termination case, if a defect such as a missing capacitor is present (this defect is shown in Figure 14) the leg with the missing capacitor will see V_{Bias} while the other leg will see a valid signal. (The unreferenced case presented both legs with a null condition.) Since test structures are to be added to both legs (see 4.6.4) they will respond in a deterministic way.

NOTE – It is assumed here that the V_{Bias} reference has low enough impedance to isolate the two legs. If this is not true, then the receiver may see signals more like the null condition.

4.6 Test Signal Implementation

In order to test the various combinations of single-ended and differential signal paths with variations on coupling, modifications have to be made to the drive and receive sides of the path.

4.6.1 Single-ended Drive

Figure 21 shows a single-ended output stage modified in the familiar way given by IEEE Std 1149.1 for test purposes. One of two signals, the normal mission signal or test data are selected for transmission by a mode signal. (This figure does not show the full detail of the Boundary-Scan register cells that supply test data.) The test data is either the content of the Update Latch (U) when executing the (DC) EXTEST instruction, or a “Test Signal” when AC testing instruction is loaded into the device. The test signal is an AC waveform suited for transmission through AC coupling. The concept here is that the single-ended driver itself is not modified.

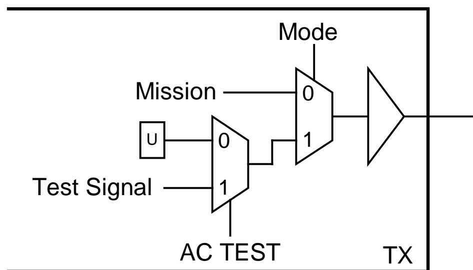


Figure 21: A single-ended driver path.

4.6.2 Differential Drive

There are two options for implementing a differential driver when incorporating test. The first is shown in Figure 22 where the selection between test and mission data is performed before the conversion to differential signaling. This means there will be only one data stream presented to the two differential pins and that the data will be transmitted in true differential form, using either current or voltage modes of the driver in question. Due to aggressive performance requirements in some higher-speed driver designs, it is expected that this option will often be chosen.

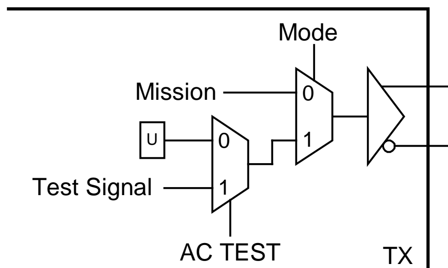


Figure 22: Full differential driver for both mission and test modes.

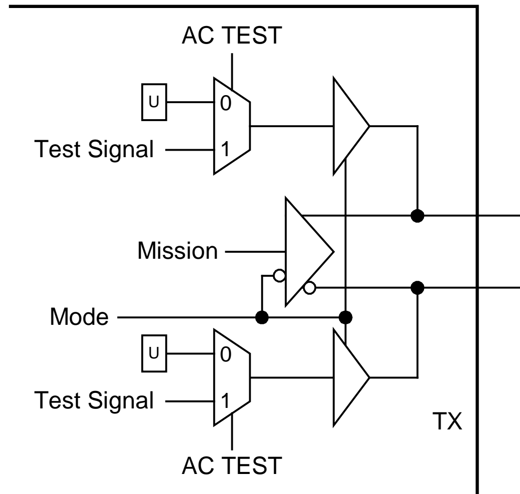


Figure 23: Differential mission/Single-ended test mode driver.

A second option for implementing testability in a differential driver is shown in Figure 23. In this case the mission mode signal path is differential, while in test mode the mission driver is disabled and two single-ended drivers with independent test data sources are enabled. Each controls a single side of the differential signal path. During test, the path is now a pair of independent single-ended signals. The two new single-ended test drivers must have similar drive characteristics as the mission driver to assure they are compatible with the loading and coupling that the mission driver would encounter.

NOTE 1 – In describing this case in BSDL (see section 7.2) the *test mode* of the driver signals are described which are single ended. Thus the signal pair is *not* described as differential. (See the "Grouped Port Identification" section B.8.8 in IEEE Std 1149.1-2001.)

NOTE 2 – If such a device supports IEEE Std 1149.4, then the structure in Figure 23 may be implemented, but with drivers of insufficient drive capacity to drive the load impedance. In this case, a hybrid of Figure 22 and Figure 23 may be implemented where AC testing operates using the model in Figure 22.

This option has desirable testability and diagnosibility features in that it removes some of the redundancy inherent in differential signaling, but it also reduces some of the noise immunity that differential signaling affords and may generate more noise during testing since the test signals on the two legs are no longer balanced and offsetting. There is additional cost in that the drive specifications (slew rate and amplitude) for the two added drivers must be substantially similar to those of the mission driver, into the mission load. There may be unacceptable mission performance degradation with this approach that makes it the less commonly chosen option.

4.6.3 Single-ended Test Signal Reception

Figure 24 shows two options for single-ended test signal reception, again familiar from IEEE Std 1149.1, but with a provision for detecting an AC test signal when an AC testing instruction is loaded in the device. When an AC testing instruction is loaded, a specialized test receiver (see 4.7) digitizes the test signal seen at the input and a detector block (Det) determines if this represents a '0' or '1'. When EXTEST is loaded, the mission signal is passed from the output of the test receiver to the Boundary Register cell. One option shown in Figure 24 supports INTEST (control and observe capability) and the other uses a simpler observe-only structure that will not support INTEST.

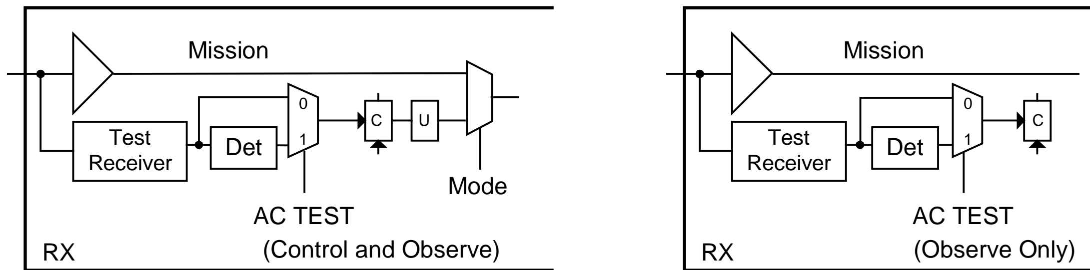


Figure 24: Choices for single-ended signal reception, with and without support for the INTEST instruction.

NOTE – The test receiver may be connected to the output of the mission input amplifier if it is a true amplifier (e.g., unity gain) rather than a threshold comparator. The test receiver is intended to process the actual waveform seen at the input pin, not an interpretation of the waveform.

A single-ended receiver has some form of reference used to distinguish a '0' from a '1' and this feature is used during (DC) EXTEST as well. However during AC testing, the signal may decay to some intermediate value that cannot be reliably received by the mission receiver. The test receiver is used to sense the AC test signal.

4.6.4 Differential Test Signal Reception

A differential receiver is modified for testability as shown in Figure 25. The mission differential receiver path is modified to capture test data seen by the mission receiver in differential mode. The mission receiver itself is unmodified.

NOTE – As shown, the mission receiver path supports INTEST, but an observe-only structure can be used instead if INTEST is not supported.

Each leg of the differential signal path has its own added test receiver. The purpose of this receiver is to monitor a leg of the signal path independently. This gives additional defect detection and diagnosis capability.

NOTE – No variations in the test receiver are needed for INTEST support since this is an observe-only monitor.

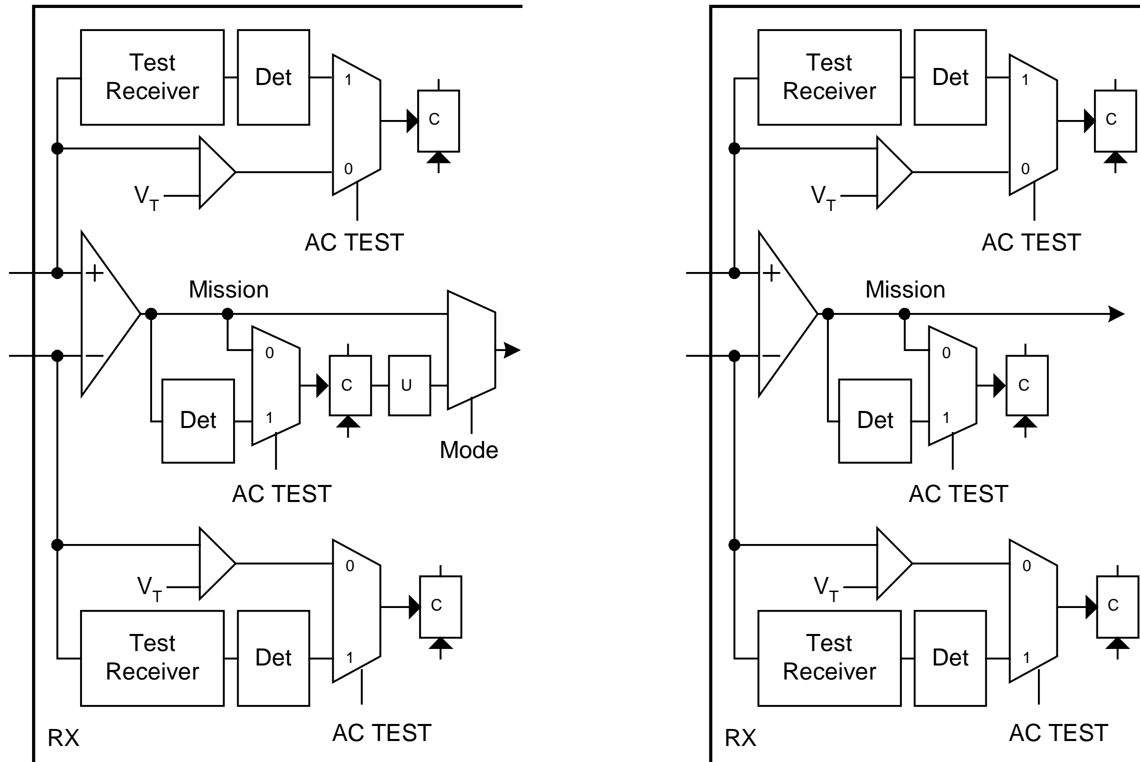


Figure 25: Differential signal reception, with and without support for the INTEST instruction.

On each leg, in addition to the test receiver, there is a fixed threshold comparator (called the “EXTEST comparator”) that compares the input waveform with a reference V_T, to produce a logical interpretation of the input. This is used for EXTEST-based testing. The value of V_T is set to the optimum common mode point of the mission receiver, which is the same as a referenced termination would use.

The EXTEST comparator is designed to produce a deterministic output when presented with a null input (both legs at the same voltage). When this receiver is AC coupled to a driver, the EXTEST instruction, when run at a low enough testing rate to fully discharge the coupling capacitors, will not be able to capture the driven data, and will thus see a null condition. This will be captured as a deterministic value. If a defect such as a shorted capacitor exists, then one of two effects will be seen:

- if the driver levels bracket the value of V_T, the driven data will be captured via the EXTEST comparator rather than a static value, or
- if the driver levels are both above or both below the value of V_T, then a static value will be produced by the EXTEST comparator that may or may not match the null default value.

These facts are useful for detecting shorted coupling capacitors. An EXTEST-based interconnect test can be constructed that causes the drivers to produce a stream of data and expects the AC coupled receivers to register a known constant value if the capacitor is not shorted.

NOTE – If the driver levels do not bracket the value of V_T, then depending on the default value picked for a null input, the shorted capacitor may produce the same value and thus not be detected. The choice of the default value should be considered with respect to possible driver technologies that might be AC coupled to this receiver to attempt to avoid this.

1 When this receiver is DC coupled to a driver and the EXTEST instruction is executed, then one of
2 two effects will be seen:

- 3 if the driver levels bracket the value of V_T, the driven data will be captured, in other
4 words, the drive levels are "close enough" to the optimum common mode voltage of the
5 receiver to register as data via the EXTEST comparator, or
- 6 if the driver levels are both above or both below the value of V_T, then a static value will be
7 observed by the EXTEST comparator, respectively a '1' or '0'.

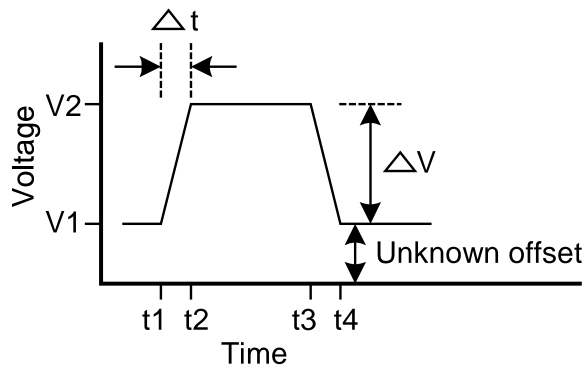
8 Thus, interconnects between DC coupled differential ICs may or may not pass data when
9 performing EXTEST. It is probable that the fact they are DC coupled indicates they will pass
10 EXTEST data. Test generation tools should examine the logic family information of the two ICs
11 to determine if this will happen.

12 NOTE – Logic family information is not included in the definition of BSDL and must come from other
13 data sheet sources.

14 Since the signals on a DC coupled differential pair may contain a significant common mode
15 offset as well as the test signal, the design of the AC test receiver must account for the fact that
16 there is no fixed reference available to discriminate a '0' from a '1'. A general discussion of the
17 test receiver is given in sections 4.7 through 4.9, and rules for its implementation are given in
18 section 6.2.

19 4.7 Test Receiver Support for AC Testing Instructions

20 The principle purpose of the test receiver seen in Figure 24 and Figure 25 is to extract a test
21 signal that may contain an offset. Because of the offset, a simple comparison of the test signal to a
22 static reference may not reliably extract the test signal. Using the opposite leg of the pair as a
23 reference (as is done by the mission receiver) will often mask important defects. A solution is to
24 look for information contained in the *transitions* of the signal. These will be independent of the
25 offset seen in Figure 26. Valid transitions have a defined voltage swing ΔV and slew rate Δt.



26 **Figure 26: A signal with unknown voltage offset and the signal transitions it contains.**

27 One way to find the transitions in a signal with an unknown offset is to compare the signal with a
28 delayed version of itself, that is, to use its recent history as a reference. This is diagramed in
29 Figure 27. The original signal, a delayed version and the output of the hysteretic comparator are
30 shown. The output is a faithful reconstruction of the original waveform, delayed by the time it
31 takes for the input waveform to pass the hysteresis threshold. The output waveform has been
32 converted to standard logic levels, that is, the unknown offset is removed.

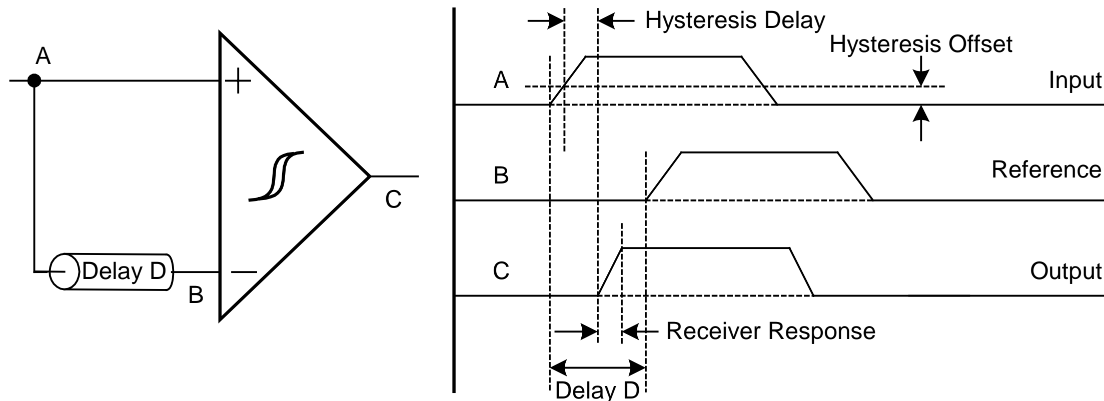


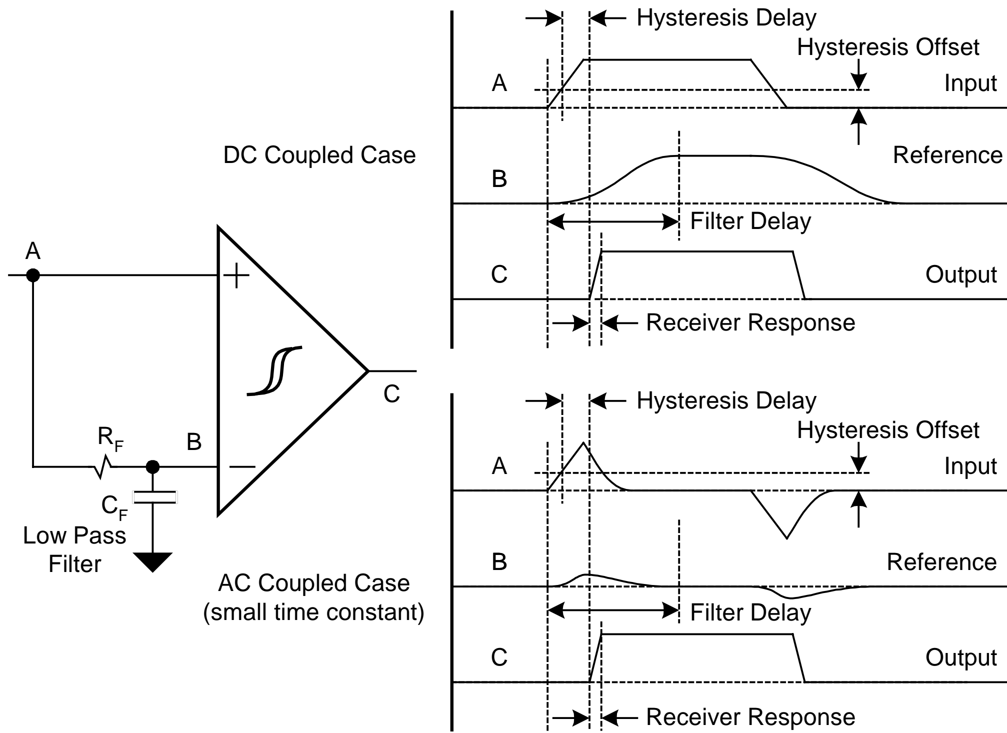
Figure 27: Delayed self-referenced reconstruction of a DC coupled input waveform with unknown voltage offset.

It will be important to assure that the delay D is longer than the transition times to be sensed. The use of hysteresis (the hysteresis voltage) can eliminate unwanted response to small signal noise (runt pulses). Additional filtering in the design of the comparator (the hysteresis delay) can eliminate response to larger signal noise of insufficient duration (noise spikes).

The waveforms that are applied to the test receiver may or may not be AC coupled to the driver. When AC coupled they may or may not decay significantly depending on the coupling time constant. In the case in Figure 27 the test receiver is either DC coupled or AC coupled with a very long time constant. If AC coupled signals with periods long with respect to the coupling time constant are applied to this simple circuit, the decaying signals will cause the comparator to reset itself early (after delay D) in response to the delayed reference edges and the reconstructed waveform will differ from the original.

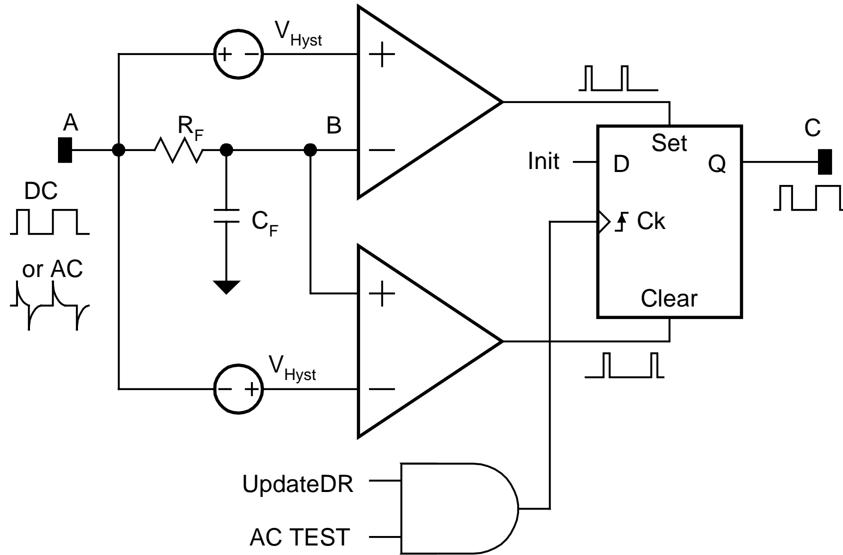
A low pass filtered delay solves this problem as shown in Figure 28. The simple low pass filter with a filtering time constant of R_F*C_F is used to hold the reference input to the test receiver at a constant value that is largely unaffected by short term events such as the high-pass filtered edges seen when AC coupling (low time constant) is used. If high time constant AC coupling, or DC coupling is used, then the low pass filter adjusts the reference point again to represent near term history of the input signal. The hysteresis voltage and hysteresis delay are used to control response to noise.

To summarize the concepts shown in Figure 28, the test receiver reconstructs an original waveform driven from either a single-ended driver or one leg of a differential driver, that is either AC or DC coupled, and is insensitive to DC offsets that may exist in the driven waveform. It does this by responding to the edges of the original waveform that are still present despite DC or AC coupling.



1 **Figure 28: Delayed and filtered self-referenced waveform reconstruction of both DC and AC coupled**
2 **waveforms by a test receiver.**

3 Figure 29 shows one possible implementation of the concept shown in Figure 28. There are two
4 simple comparators, one to sense rising edges and the other to sense falling edges. The V_{Hyst}
5 voltage sources set the hysteresis voltage for the comparators. The internal delay of the
6 comparators determine the hysteresis delay. The comparator outputs set or clear a D-type flip-
7 flop. The values of R_F and C_F are chosen to cause a delay longer than the expected transition
8 times being sensed.



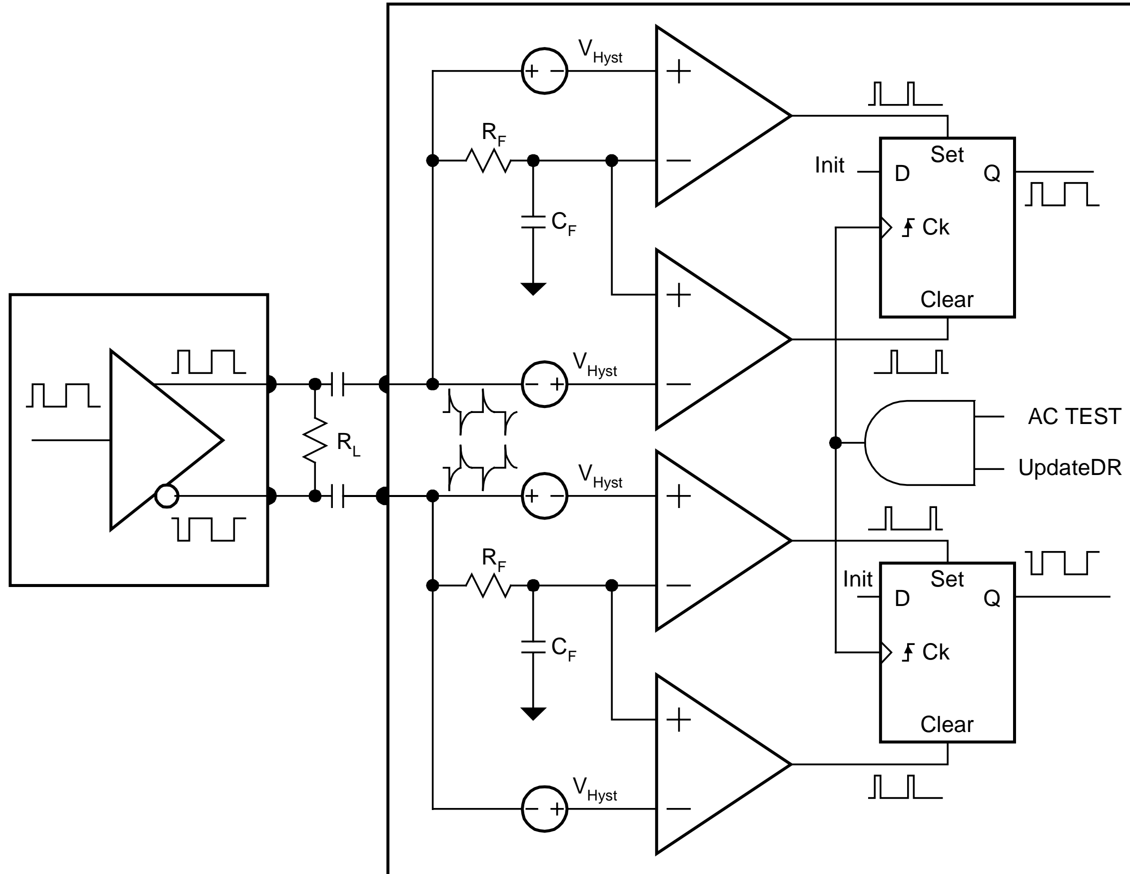
1 **Figure 29: A simple test receiver implementation possibility for the concept in Figure 28.**

2 NOTE 1 – Typical values of R_F and C_F might be 5 Kohms and 5 picofarads which could be integrated into
3 an IC.

4 NOTE 2 – The input waveform at point A may be high-pass filtered by AC coupling, or it could be a
5 normal DC coupled digital waveform (with an unknown offset). In either case, the edges are used to
6 reconstruct the original digital waveform.

7 NOTE 3 – The D-type flip-flop element can be initialized by the Update clock to establish a known initial
8 state at the time the drivers are triggered. The initialization value will be discussed later.

9 Figure 30 shows an AC coupled differential signal channel from the drive side, done
10 differentially, to the receive side which is single-ended for test purposes. (The mission receiver
11 has been omitted for clarity.) This supports the AC testing instructions.



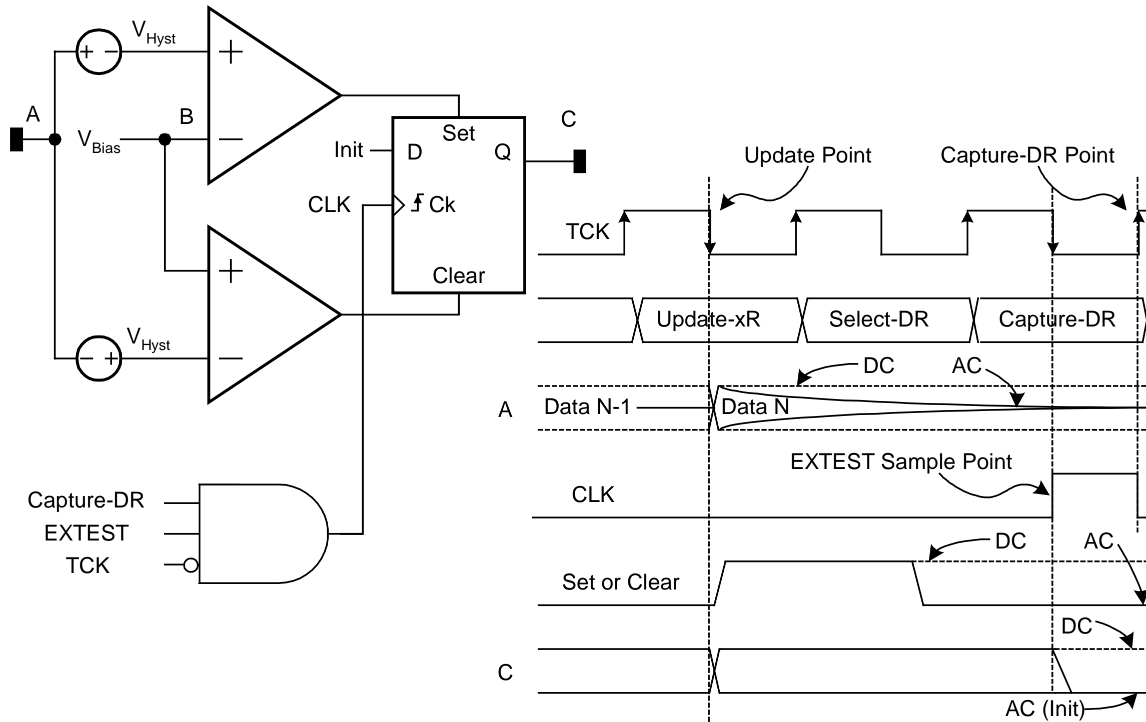
1 **Figure 30: Differential driver, AC coupling, and receiver testability structure.**

2 NOTE – In Figure 30 the mission receiver has not been shown. It would include load termination that
3 would determine the time constant of the AC coupling.

4 *4.8 Test Receiver Support for the (DC) EXTEST Instruction*

5 The test receiver behavior for AC testing has been described. However it also is important to
6 support the standard (DC) EXTEST instruction. This amounts to "turning off" the edge
7 integrating capability of the test receiver and having it respond only to levels. This is further
8 complicated by the problem that there may be common mode offsets added to the signals. This
9 necessitates choosing a reference voltage that can be used for single-ended comparison.

10 One choice is to use the internal bias voltage V_{Bias} used to set the V_{Com} point of the mission
11 receiver (the "sweet spot") as shown in Figure 31. This bias voltage will work well as a static
12 reference for the test receivers when AC coupling is used. If the receiver IC is DC coupled to the
13 driver, then the test receiver may or may not receive data depending on whether V_{Bias} is between
14 the high and low values driven by the driver. If data is not received, the test receiver will perceive
15 a constant logic value, either 1 or 0.



1 **Figure 31: Static reference used to support (DC) EXTEST. Comparators may set or reset the**
2 **hysteresis flip-flop just before the rising edge of TCK in the Capture-DR state.**

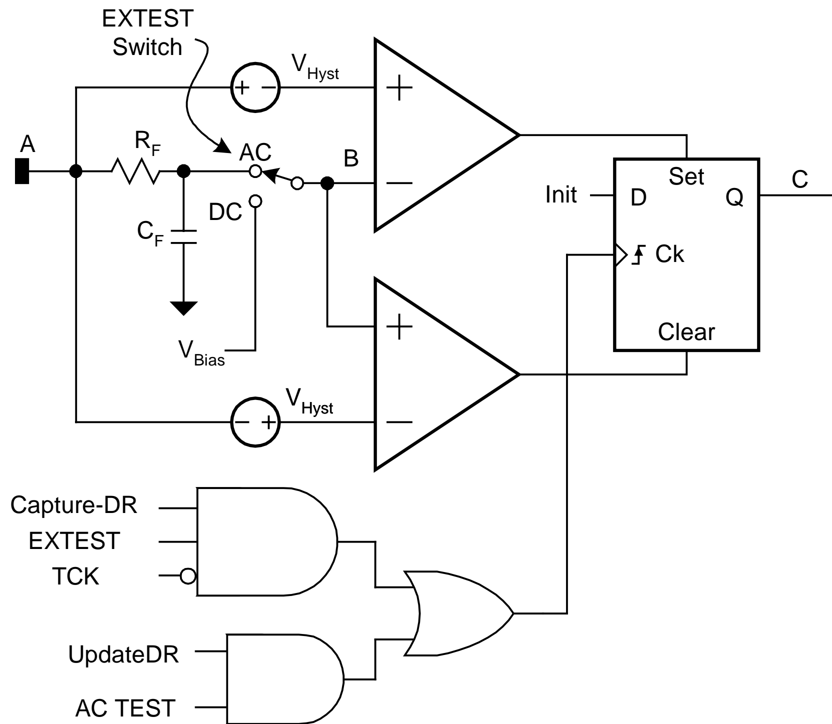
Editor's note: In the above figure, the value of V_{Hyst} should be half that used for the self-referenced comparison. This error appears throughout and needs correction.

3 If the test receiver is responding to the EXTEST instruction but the receiver is AC coupled to the
4 driver, there is the chance, particularly if the coupling time constant is longer, that the receiver
5 will respond to a change in the driven data (see waveforms in Figure 31). The flip-flop is clocked
6 falling edge of TCK in the Capture-DR state to set a default initial state. If there is a DC level on
7 the test receiver input, this will override the initial state. If the levels have decayed due to AC
8 coupling, then the initial state will not be overridden. Extra time for signal decay can be inserted
9 by spending time in the Run-Test/Idle state.

10 NOTE -- Figure 31 also demonstrates how a shorted coupling capacitor can be detected by EXTEST. A
11 shorted capacitor will prevent signal decay, overriding the default value. If the default is the opposite state
12 of the driven value, a detection is possible.

13 4.9 A General Test Receiver for DC and AC Testing Instructions

14 A test receiver that supports both the AC and (DC) EXTEST instructions is required. This could
15 be accomplished simply by taking the two structures already shown and selecting between them
16 with multiplexers. However it is possible to merge their behaviors into a more efficient structure
17 as shown in Figure 32. In this structure an analog multiplexer selects between (DC) EXTEST
18 support and AC testing support.



1 **Figure 32: A test receiver structure that supports both AC and (DC) EXTEST.**

2 ## *4.10 Boundary-Scan Capture Data Versus Configuration*

3 The content of Table 2 shows what Boundary-Scan data will be captured by a test receiver for
4 various combinations of coupling, DC compatibility and whether a given IC is executing
5 EXTEST or an AC testing instruction.

6

Table 2: Boundary-Scan capture results for various combinations of coupling, test instruction and driver-to-receiver DC compatibility.

Driver to Receiver Coupling	Test instruction loaded in:		Capture result when DC levels of driver and receiver are:		Comments
	Driving IC	**Receiving IC**	**Compatible**	**Incompatible**	
DC	EXTEST		Data (Note 1)	Fixed 1 or 0 (Note 2)	Typical test for DC coupling.
DC	AC Test		Data		AC test on DC coupled paths may be forced by board topology.
DC	EXTEST	AC Test	Data/Default		Driver does not get its “throat cleared” because it is in EXTEST. Data is transmitted when it differs from the last applied data, otherwise the default is received, but there is greater noise vulnerability.
DC	AC Test	EXTEST	Data	Fixed 1 or 0	
AC	EXTEST		Default (Note 3)		Used to test shorted capacitors. Will pass data (a failure) or will register a (possibly passing) default value.
AC	AC Test		Data		Typical test for AC coupling.
AC	EXTEST	AC Test	Data/Default		Driver does not get its “throat cleared” because it is in EXTEST. Data is transmitted when it differs from the last applied data, otherwise the default is received, but there is greater noise vulnerability
AC	AC Test	EXTEST	Default		May be used to test shorted capacitors.

NOTE 1 – In Table 2, “data” indicates Boundary-Scan data is successfully transmitted.

NOTE 2 – “Fixed 0 or 1” indicates the incompatible levels will be seen as either a 1 or 0 depending on where the receiver threshold is set.

NOTE 3 – “Default” indicates the response is the same that a floating test receiver would produce.

1 ### *4.11 Noise Sources and Sensitivities*

Editor's Note: The following section will discuss the sources of noise, how the Test Receiver is sensitive to noise, and how to avoid susceptibility. This will offer guidance to IC designers, board designers, and test engineers. Rules that appear in later clauses will specify Test Receiver noise characteristics relative to the mission mode of the system. Not clear if we can impose rules on board designers or test engineers.

2

3 #### 4.11.1 Noise Sources that Affect Mission Operation

4 Ground bounce, signal coupling, EMI

5 #### 4.11.2 Noise Sources Unique to Testing

6 Intra-IC noise generation (lobotomy effect), rogue signals on the board, impedance mismatches

7 #### 4.11.3 Noise Sources Exacerbated by Testing

8 Ground bounce, signal coupling

9 #### 4.11.4 Avoiding Noise

10 Hysteresis voltages, hysteresis delay, self-reference filtering, use of the Run-Test/Idle state, noise
11 rejection of the data protocol, limits on ATPG

12

1 # 5 TAP Instructions

2 ## 5.1 IEEE Std 1149.1 Instructions

3 All TAP instructions provided by IEEE Std 1149.1 perform as specified in that standard for all
4 DC pins. For AC pins, all IEEE Std 1149.1 instructions perform as specified with the exception
5 of the introduction of hysteresis behavior for AC input pins. (See section 6.2.2.)

6 ### 5.1.1 Rules

7 a) All instructions specified by IEEE Std 1149.1 shall perform as specified in that standard,
8 and for any such instruction that controls or observes pins, all DC pins shall also perform
9 as specified by that standard.

10 NOTE – The AC pins shall perform per rules specified herein.

11 ### 5.1.2 Description

12 The IEEE Std 1149.1 standard is the foundation for this standard. The (DC) EXTEST instruction
13 enables level-detecting behavior (see section 6.2.2) on signal paths containing AC pins. This
14 instruction is useful for detecting shorted capacitors on AC coupled paths.

15 ## 5.2 AC Testing Instructions

16 This standard mandates the addition of two new instructions that generate and process an AC test
17 signal. This signal modulates test data so that it will propagate through AC coupled channels, for
18 devices that contain AC pins. The first is EXTEST_PULSE (see 5.3) and the second is
19 EXTEST_TRAIN (see 5.4). These instructions are similar in that they both generate an AC test
20 signal, and differ in the details of the AC test signal that each generates. The AC test signal is
21 distributed to each AC pin that contains a driver.

Editor's Note: I have left the door open here for:
1. A device with zero AC pins not implementing AC Testing instructions, and
2. Other instructions we may decide to implement (e.g, for I/O configuration

22 ## 5.3 The EXTEST_PULSE Instruction

23 This standard specifies a new test mode instruction, EXTEST_PULSE, which governs new
24 capabilities defined for AC pins (see 4.1). All DC pins will perform as if the IEEE Std 1149.1
25 EXTEST instruction is operating whenever the EXTEST_PULSE instruction is effective.

26 ### 5.3.1 Rules

27 An EXTEST_PULSE instruction shall be provided for components that possess AC pins, and
28 the component designer shall select the opcode(s) for this instruction.

29 a) The EXTEST_PULSE instruction shall become effective at the falling edge of TCK in
30 the *Update-IR* TAP Controller state.

31 NOTE – By "effective" it is meant that (enabled) AC drive pins shall respond to the content of the
32 Boundary Scan register as specified in section 6.3.2, and AC receive pins shall behave as specified in
33 section 6.2.3.

b) The EXTEST_PULSE instruction shall remain effective in the *Run-Test/Idle* TAP Controller state.

c) DC pins shall perform exactly as specified for the EXTEST instruction by IEEE Std 1149.1 whenever the EXTEST_PULSE instruction is effective.

d) When a device contains AC pin with drivers, the EXTEST_PULSE instruction shall generate an "AC Test Signal" with these characteristics:

   i. the AC Test Signal shall be forced to the de-asserted state in the *Test-Logic-Reset* TAP controller state, and

   ii. the AC Test Signal shall transition to the asserted state on the first falling edge of TCK in the *Run-Test/Idle* TAP controller state, and

   iii. the AC Test Signal shall transition to the de-asserted state on the first falling edge of TCK after leaving the *Run-Test/Idle* TAP controller state, and

   iv. the AC Test Signal shall not change at any other time.

NOTE – The AC Test Signal is used only by AC pin drivers as specified in section 6.3.2. If a device does not contain AC pin drivers, then the AC Test Signal does not need to be generated.

5.3.2 Description

The EXTEST_PULSE instruction implements new test behaviors for AC pins, and simultaneously behaves identically to IEEE Std 1149.1 EXTEST for DC pins. (See Clause 6 for the specification of AC test behavior.)

The EXTEST_PULSE instruction enables edge-detecting behavior (see section 6.2.3) on signal paths containing AC pins, where test receivers reconstruct the original waveform created by a driver even when signals decay due to AC coupling.

The EXTEST_PULSE instruction, by action of the AC Test Signal, causes data produced by drivers (see 6.3.2) to be inverted on the first falling edge of TCK after entering the *Run-Test/Idle* TAP controller state, and to be restored on the first falling edge of TCK after leaving this state as shown in Figure 33. This generates a pulse of inverted data on a driver that is as wide as the time spent in the *Run-Test/Idle* TAP controller state. If the *Run-Test/Idle* TAP controller state is not entered, then the EXTEST_PULSE instruction is not distinguishable from the (DC) EXTEST instruction.

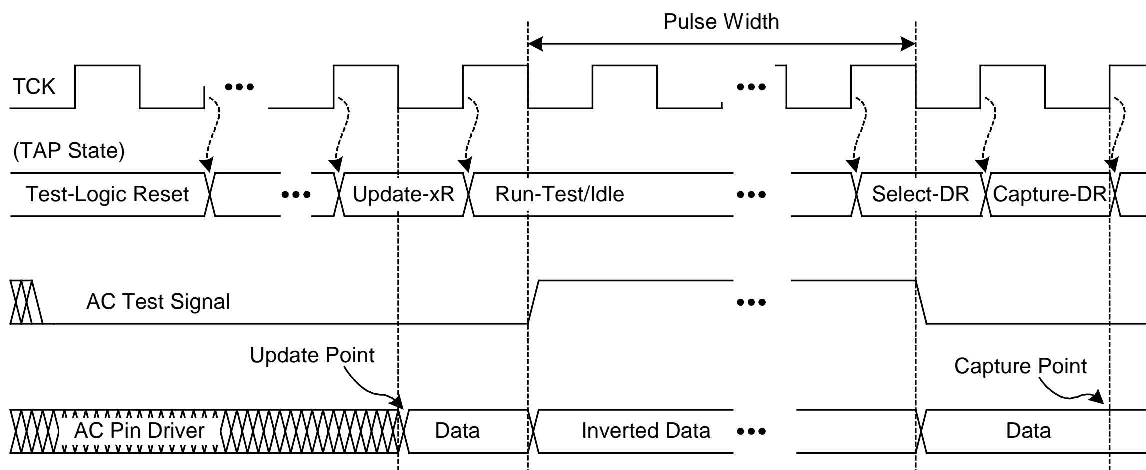


Figure 33: Behavior of (active high) AC Test Signal when EXTEST_PULSE is effective.

5.4 The EXTEST_TRAIN Instruction

This standard specifies a new test mode instruction, EXTEST_TRAIN, which governs new capabilities defined for AC pins (see 4.1). All DC pins will perform as if the IEEE Std 1149.1 EXTEST instruction is operating whenever the EXTEST_TRAIN instruction is effective.

5.4.1 Rules

a) An EXTEST_TRAIN instruction shall be provided for components that possess AC pins, and the component designer shall select the opcode(s) for this instruction.

b) The EXTEST_TRAIN instruction shall become effective at the falling edge of TCK in the *Update-IR* TAP Controller state.

NOTE – By "effective" it is meant that (enabled) AC drive pins shall respond to the content of the Boundary Scan register as specified in section 6.3.2, and AC receive pins shall behave as specified in section 6.2.3.

c) The EXTEST_TRAIN instruction shall remain effective in the *Run-Test/Idle* TAP Controller state.

d) DC pins shall perform exactly as specified for the EXTEST instruction by IEEE Std 1149.1 whenever the EXTEST_TRAIN instruction is effective.

e) When a device contains AC pin with drivers, the EXTEST_TRAIN instruction shall generate an "AC Test Signal" with these characteristics:

   i. the AC Test Signal shall be forced to the de-asserted state in the *Test-Logic-Reset* TAP controller state, and

   ii. the AC Test Signal shall transition to the asserted state on the first falling edge of TCK in the *Run-Test/Idle* TAP controller state, and

   iii. the AC Test Signal shall invert its state on subsequent falling edges of TCK while still in the *Run-Test/Idle* TAP controller state, and

   iv. the AC Test Signal shall transition to the de-asserted state on the first falling edge of TCK after leaving the *Run-Test/Idle* TAP controller state if it was asserted just before leaving, and

   v. the AC Test Signal shall not change at any other time.

NOTE – The AC Test Signal is used only by AC pin drivers as specified in section 6.3.2. If a device does not contain AC pin drivers, then the AC Test Signal does not need to be generated.

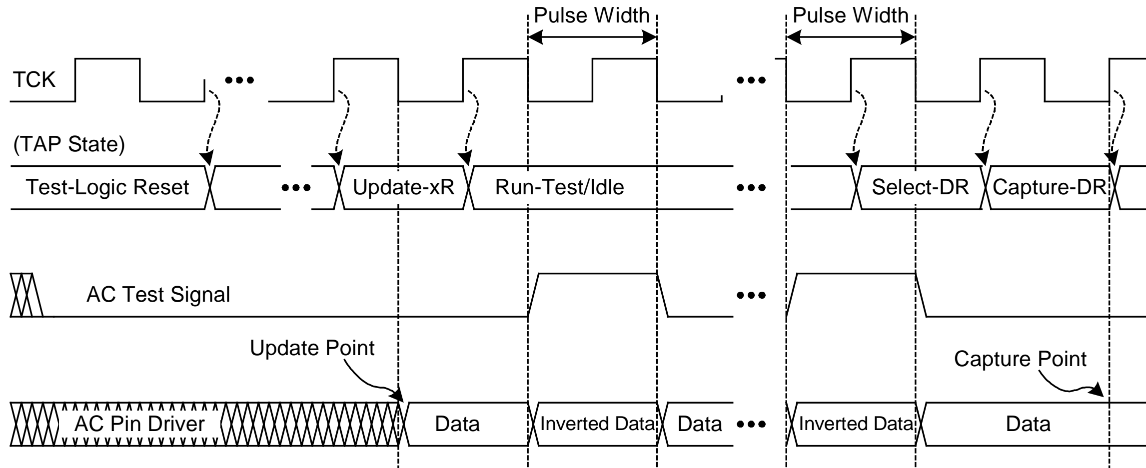
5.4.2 Description

The EXTEST_TRAIN instruction implements new test behaviors for AC pins, and simultaneously behaves identically to IEEE Std 1149.1 EXTEST for DC pins. (See Clause 6 for the specification of AC test behavior.)

The EXTEST_TRAIN instruction enables edge-detecting behavior (see section 6.2.3) on signal paths containing AC pins, where test receivers reconstruct the original waveform created by a driver even when signals decay due to AC coupling.

The EXTEST_TRAIN instruction, by action of the AC Test Signal, causes data produced by drivers (see 6.3.2) to be inverted on the first falling edge of TCK after entering the *Run-Test/Idle* TAP controller state, and to be subsequently toggled on each falling edge of TCK while remaining in this state as shown in Figure 34. This generates a rectangular wave on a driver, each full cycle being two cycles of TCK wide. The first falling edge of TCK after leaving the *Run-Test/Idle* TAP controller state will restore driver data if it is not already matching the value in the Update flip-flop. If the *Run-Test/Idle* TAP controller state is exited after only one cycle of TCK,

1 then the EXTEST_TRAIN instruction is not distinguishable from the EXTEST_PULSE
2 instruction. If the *Run-Test/Idle* TAP controller state is not entered, then the EXTEST_TRAIN
3 instruction is not distinguishable from the (DC) EXTEST instruction.



4 **Figure 34: Behavior of (active high) AC Test Signal when EXTEST_TRAIN is effective.**

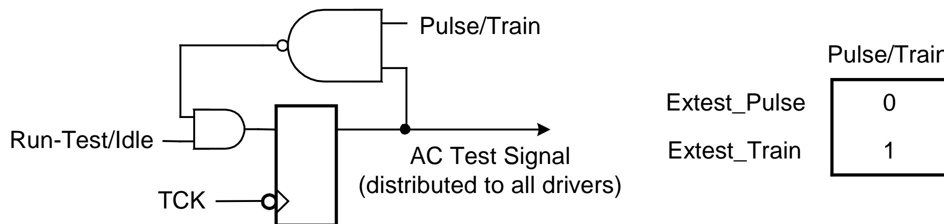
5 NOTE 1 – Depending on when the *Run-Test/Idle* TAP controller state is exited (on an even or odd count of
6 TCK) there may be an extra half cycle of time where AC Test Signal is held low.

7 NOTE 2 – If, as allowed by IEEE Std 1149.1, TCK is halted, a pulse or time between pulses may be
8 stretched.

9 ## 5.5 AC Test Signal Generation

10 A possible implementation of AC Test Signal generation is shown in Figure 35, for both the
11 EXTEST_TRAIN and EXTEST_PULSE instructions. This circuit would probably be located
12 near the TAP controller since it uses decoded information (e.g., RTI State and Pulse/Train) from
13 the TAP controller to generate the global AC Test Signal.

14 It is not necessary (indeed perhaps undesirable) to propagate the AC Test Signal to all drivers
15 with minimal skew, as long as the skew accumulated across the device stays under ½ of a TCK
16 cycle. Skew will cause drivers to respond at slightly different intervals to the AC Test Signal,
17 which will reduce power supply fluctuations and related noise when many AC drivers are so
18 controlled.



19 **Figure 35: Circuitry to generate a global AC Test Signal.**

1 # 6 Pin Implementation Specifications

2 ## 6.1 Pin Identification

3 The device designer is expected to survey the complete set of pins of the device and categorize
4 them as:

5 - Power/ground and other analog reference pins
6 - TAP signal pins (per IEEE Std 1149.1-2001, clause 4, “The Test Access Port”)
7 - Compliance enable pins (per IEEE Std 1149.1-2001, section 4.8, “Subordination of
8 this standard within a higher level test strategy”
9 - DC pins, I/O signal pins specifically addressed by IEEE Std 1149.1-2001
10 - AC pins, I/O signal pins that are expected by design to support AC coupling to other
11 signal pins. Note this coupling may or may not be used in a given board application.

12 Thus a designer can partition pins into those traditionally governed by IEEE Std 1149.1-2001 and
13 those additionally governed by this standard (i.e., AC pins).

14 ### 6.1.1 Rules

15 a) The device designer shall enumerate a [possibly empty] set of device signal pins that can
16 support AC coupled signaling to and/or from other pins and shall designate these pins
17 “AC pins”.

18 b) The device designer shall categorize all other device pins per the rules in IEEE Std
19 1149.1-2001.

20 NOTE – Those I/O signal pins so identified are herein called “DC pins”.

21 ### 6.1.2 Description

22 The device designer effectively partitions the I/O signals into those addressed only by IEEE
23 1149.1-2001 and those (AC pins) addressed by this standard.

24 [The set of AC pins may be empty if other features (TBD??) of this standard are implemented but
25 no AC coupling is supported.]

26 ## 6.2 Input Test Receivers

27 All AC pins (see 4.1) that receive data into an IC are equipped with test receivers. Single-ended
28 AC pins will have one test receiver and differential channels will have one test receiver per leg.
29 The IC designer will design the mission performance of the input to accept some range of voltage
30 changes and slew rates. The rules given below assume that an input will respond to a minimum
31 input voltage change and that the slew rate of input changes will be at or above some minimum,
32 because AC coupling is anticipated or even built into the IC itself. These minimums are defined
33 by the performance requirements of the mission of the IC and are depicted in Figure 36 for both
34 AC and DC coupled signals.

35 When an AC testing instruction is in effect, it is the purpose of the test receiver to reconstruct the
36 test waveform driven by the upstream driver when either AC or DC coupling is used. It does this
37 by reacting to the edges and not the levels of the input waveform. When (DC) EXTEST is in
38 effect, the test receiver behaves as a level detector.

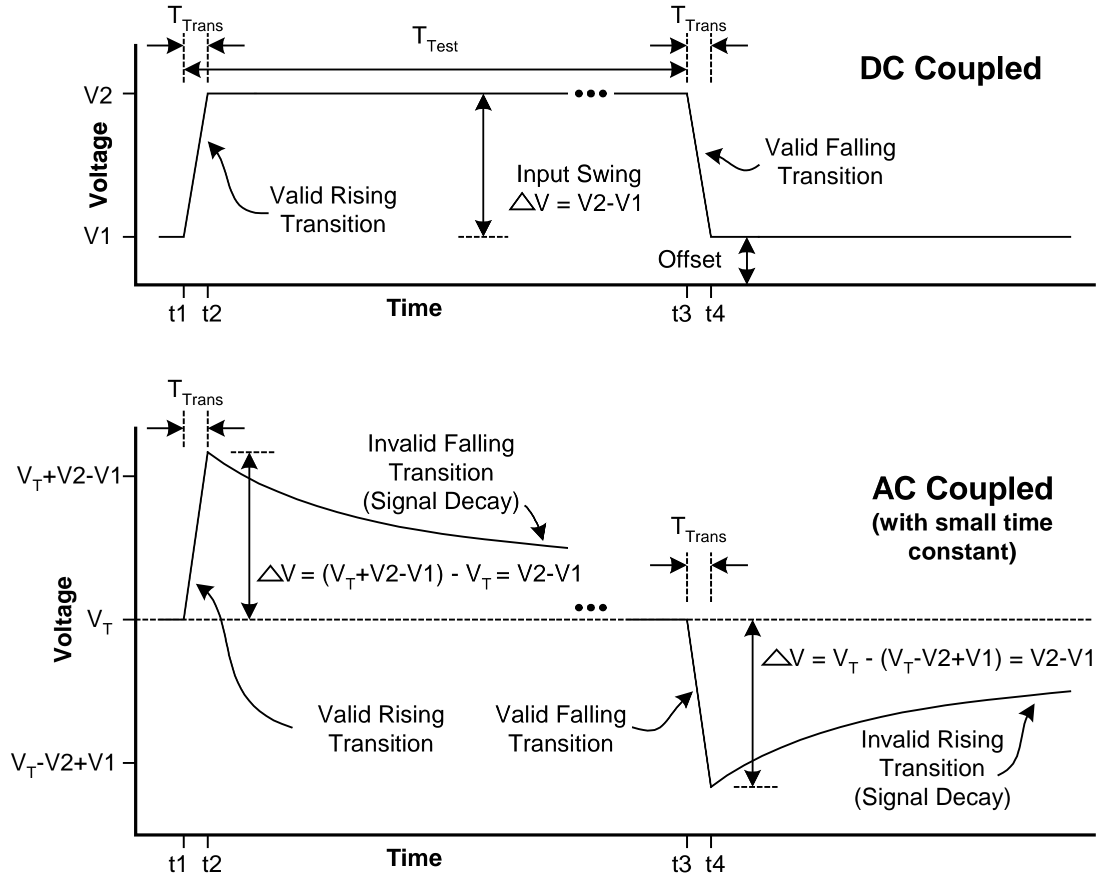


Figure 36: Definitions of voltage changes and transition times for waveforms presented to the test receiver using either DC or AC coupling.

The value of T_{Test} is the minimum time between signal transitions that can be caused by Boundary-Scan testing. This value is governed by test-related parameters such as TCK frequency for the device (for EXTEST_TRAIN) or the time spent in *Run-Test/Idle* (for EXTEST_PULSE).

NOTE – IEEE Std. 1149.1 EXTEST does not take attenuation or transition time into account. The test transitions are very far apart (at best, once per scan and update of the boundary register). Receiver values are captured no sooner than 2.5 TCK cycles after a possible transition.

The *minimum input swing*, termed ΔV_{Min}, is the smallest change in voltage during an active transition (ΔV in Figure 36) that is expected to occur during tests specified by this standard. Typically, this will be the ΔV_{Min} of a driver of the same protocol and technology reduced by some factor to account for attenuation expected at the maximum test frequency ($1/(2*T_{Test})$ in Figure 36). This attenuation is generally significantly less than the attenuation expected at maximum functional channel frequency. The transition time, T_{Trans} in Figure 36, is the maximum amount of time this minimum voltage swing is expected to take. Signal transitions that take significantly longer than T_{Trans} are not considered valid. For example in Figure 36, the passive, undriven, falling decay on a capacitively coupled signal that follows an actively driven rising transition is not a valid falling transition. The rules that follow will define a test receiver that can differentiate a valid signal transition from a decay transition.

In the following rules, a designer is required to identify parameters such as minimum and maximum voltage swing (ΔV_{Min}, ΔV_{Max}) and maximum transition time (T_{Trans}), but with some latitude.

The preferred way to determine these parameters is to start with the transmission protocol specification. For example, the LVDS Standard (IEEE Std 1596.3, or ANSI/TIA/EIA-644) specifies that the voltage swing at the driver should be 454mv maximum and 247mv minimum. It also states the voltage swing at the receiver should be 100mv minimum, but this is at maximum data rate, as shown in Figure 37. The standard does not state an expected attenuation at a slower test data rates, e.g., 5 - 50MHz, but conservative engineering judgement might suggest that the minimum voltage swing at the receiver, for that frequency, would be no less than, for example, 80% of the minimum swing at the driver, or about 200mv in this example. The maximum swing of the driver (454mv) could then be used as ΔV_{Max} and the attenuated minimum swing of the driver (200mv) used as ΔV_{Min}.

The LVDS standard further specifies a maximum driver transition time of 1.5ns for data rates greater than 200Mbps, or 30% of the bit-width otherwise. The standard documented here provides that the transition time of the driver is the same in test mode as in functional operation, so one should be able to use this same value for test. However, the transition time at the receiver will be longer than the transition time at the driver due to high frequency attenuation, even in low data-rate operation. So at the receiver, a better estimate for T_{Trans} would be 50% of the minimum bit time (25% of the maximum channel frequency cycle time) since longer transition times than that would cause severe amplitude attenuation at the maximum data rate and probably compromise the reliability of the channel. To continue the example, assume an LVDS driver and receiver designed for 200Mbps maximum bit rate, then the bit time would be 5ns. The LVDS Standard dictates 30% of the bit time, or 1.5ns, for the driver transition time, and for this Standard one could use 50% of the bit time, or 2.5ns, for the receiver transition time called T_{Trans}.

When there is no other guidance, a possible way to determine these parameters is to consider the actual characteristics of a driver implemented in the same technology for the same channel protocol. Over acceptable manufacturing process variation, temperature variation, etc, this driver will produce a maximum and a minimum voltage swing into a specified range of loads. This voltage swing will normally be larger than needed to assure the receiver reliably recovers data, to allow for high frequency attenuation in the channel between the driver and receiver (see Figure 37). As described above for the LVDS example, a conservative attenuation factor for the maximum expected test frequency can be determined using appropriate engineering tools and judgement and applied to the minimum voltage swing to determine an appropriate minimum voltage swing during test at the test receiver. (The maximum voltage swing is not usually adjusted to allow for very tight coupling with negligible attenuation.)

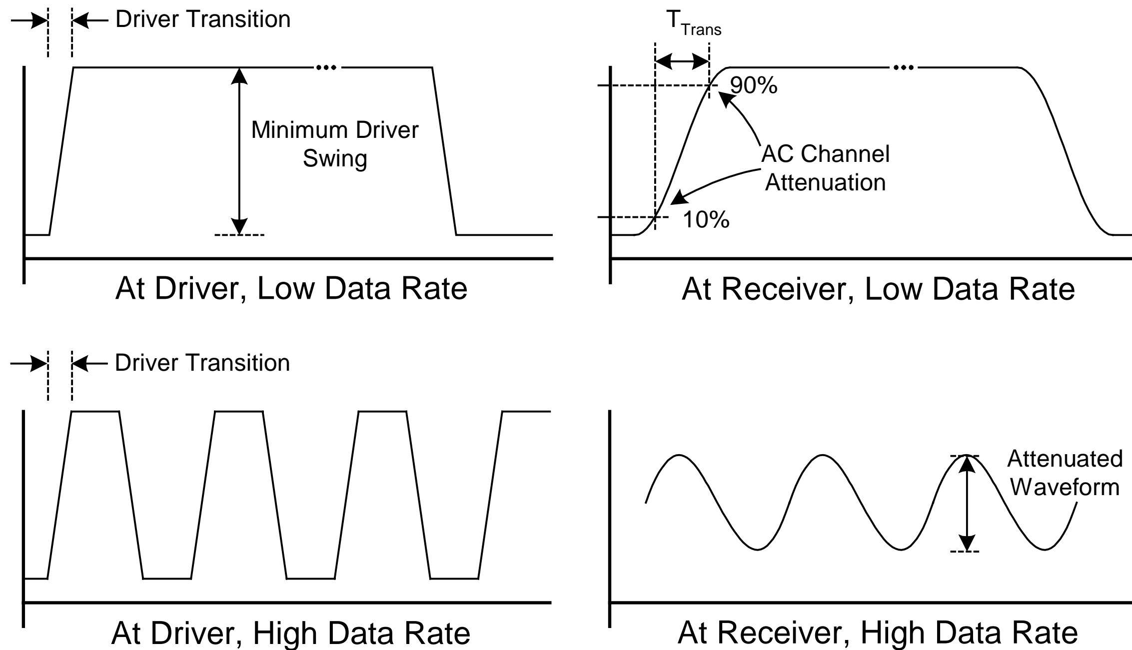


Figure 37: Driver waveform and the attenuated waveform seen at the receiver. The attenuation is a function of driver data rate.

In addition, both driver and receiver will be designed for a specific maximum channel frequency or bit width. Again, a good estimate for T_{Trans} at the receiver, in a typical channel design, would be 50% of the bit width or 25% of the cycle time at maximum frequency.

If the designer is expecting the receiver to be connected, AC or DC coupling, to a driver of a different transmission protocol, or implemented in a different technology, then analysis of the board channel design will have to be performed to verify that the channel will attain the desired data rate. By extending this analysis, using the techniques described above, the designer can determine the required parameters.

These types of considerations allow the designer to define the minimum and maximum voltage swings and transition time required by the following rules. This "test design point" information may be supplied as part of the data sheet for the final device.

The offset voltage shown in Figure 36 may vary depending on different circuit configurations. For example, an IC with an input pin possessing a test receiver may be AC or DC coupled to a driver intentionally by a board designer. Depending on which is chosen, there could be different offsets observed at the test receiver. When a defect occurs, the coupling may be affected. For example, a shorted coupling capacitor may create DC coupling to a receiver that was intended to be AC-coupled.

6.2.1 General Properties of AC Input Pins and Test Receivers

6.2.1.1 Rules

a) All AC pins (see 4.1) that receive input data, whether they are single-ended or part of a differential pair, shall have a test receiver function monitoring the pin.

NOTE – This rule applies to input and bidirectional pins (see AC pin definition in section 4.1).

b) With respect to the required or expected mission behavior of the input signal at an AC input pin, the device designer shall identify a *minimum valid signal transition* in terms of

its *minimum input swing* (ΔV_{Min}) and *maximum transition time* (T_{Trans}) over which this minimum input swing may occur.

NOTE 1 – In the event that the pin is one-half of a differential pair, the determination of ΔV_{Min} is with respect to a fixed reference (e.g., ground) and not with respect to the other member of the differential pair.

NOTE 2 – If the transition times of rising and falling edges are different, then the longer of the two is defined as the maximum.

NOTE 3 – See permission 6.2.1.2c) for the case where there is no maximum transition time specification for the mission receiver. See also the discussion in section 6.2 on determining T_{Trans}.

c) With respect to the required or expected mission behavior of the input signal at an AC input pin, the device designer shall identify a *maximum valid signal transition* in terms of its *maximum input swing* (ΔV_{Max}).

NOTE – If the pin is bidirectional, then the pin driver may determine ΔV_{Max}, but some external, AC attenuated driver may determine T_{Trans}.

d) The test receiver shall be implemented to operate in two modes of operation:
   i. a level-detecting mode selected by the (DC) EXTEST instruction (see specifications in section 6.2.2), and
   ii. an edge-detecting mode selected by an AC testing instruction (see specifications in section 6.2.3).

e) The test receiver shall be implemented with hysteresis voltage offsets for the two operational modes called:
   i. V_{Hyst_Level} in the level-detecting mode (see detail in section 6.2.2), and
   ii. V_{Hyst_Edge} in the edge-detecting mode (see detail in section 6.2.3).

6.2.1.2 Permissions

a) A test receiver may be isolated from its pin with a linear buffer as long as it still sees the actual waveform appearing on the pin.

b) Circuitry needed to implement the test receiver may be shared with that needed for the implementation of the mission circuitry, as long as all rules for this standard are observed.

c) If the mission receiver has no specification for a maximum transition time, then the value of T_{Trans} may be chosen to match the maximum expected transition time for an upstream driver that is in test mode, taking into account any expected AC attenuation in the path.

NOTE – See the discussion in section 6.2 on determining T_{Trans}.

6.2.1.3 Description

The rules and permissions in Section 6.2.1 require that there be a bimodal test receiver on each and every AC input pin, and define five electrical parameters based on the expected mission-mode input signal, that shall be used to design the test receiver. Consider rule 6.2.1.1b). This rule applies to signal transitions within any common mode or fixed voltage range definition of the mission of the pin. Changes outside of this range are not valid signal transitions. For example, a signal transition that forward biases input protection diodes would be outside the normal operating range of the receiver. In addition, the minimum valid signal transition is the smallest, slowest transition that represents a valid state change of the signal, i.e., that represents a change in signal data (and is to be differentiated from a signal decay seen in an AC coupled channel). This could be determined by examining the characteristics of a driver implemented in the same technology, its minimum specifications, and the maximum amount of signal attenuation allowed between the driver and receiver. The transition parameters (T_{Trans} and ΔV_{Min}) are used in subsequent rules.

Permission 6.2.1.2c) allows a device designer to substitute the maximum transition time of an upstream driver in test mode that is expected to be connected to this test receiver. This handles the case where there is no maximum transition time specified for the mission receiver, for example, a low frequency analog input. A designer can thus avoid having to implement edge-detection for very slow edges. However the designer must assure that the upstream driver's parameters are known, which is often the case for custom designs or standard logic families.

Rule 6.2.1.1c) defines a maximum input voltage swing. This value, the tolerable amount the receiver can be overdriven, is used in subsequent rules to improve the noise immunity of the test receiver.

Rule 6.2.1.1d) requires that the test receiver have a level-detection mode (familiar from IEEE Standard 1149.1) and also an edge-detecting mode. The edge-detecting mode is required since AC coupling is a high-pass filter that will not propagate DC levels.

Rule 6.2.1.1e) states the test receiver will be implemented with voltage hysteresis levels, with a specification for level and edge detecting modes. While this hysteresis provides noise immunity, it also defines the test receiver as having three possible detection states: legal "one", legal "zero", and an "indeterminate" value in between. Due to the behavior of DC signals when transmitted on an AC-coupled net, the explicit detection of the "indeterminate" input state is critical to defect detection and diagnosis. More specifications on edge and level detection are given in the following sections as a function of these hysteresis parameters.

6.2.2 Level Detection Behavior of Input Test Receivers

The level detection behavior is selected by the (DC) EXTEST instruction from IEEE Std 1149.1.

6.2.2.1 Rules

a) For the level-detection mode of a test receiver, the device designer shall identify a fixed threshold voltage $V_{Threshold}$ that defines the mid-range of the minimum input voltage swing ΔV_{Min}, and the designer shall identify a hysteresis voltage offset value V_{Hyst_Level}.

b) Whenever a test receiver is operating in level-detection mode on an AC input pin, the test receiver shall:

   i. determine the logic value on the pin by comparing the current voltage on the pin to a fixed threshold voltage $V_{Threshold}$ for a minimum period of time called the hysteresis delay (T_{Hyst}) and,

   ii. output a logic one only after this period has elapsed and if the voltage continuously compares greater than this threshold $V_{Threshold}$ plus the hysteresis voltage V_{Hyst_Level} or,

   iii. output a logic zero only after this period has elapsed and if the voltage continuously compares less than this threshold $V_{Threshold}$ minus the hysteresis voltage V_{Hyst_Level}.

c) The device designer shall choose the delay period (THyst) by considering recommendation 6.2.2.3a).

d) Whenever a test receiver is operating in the level-detection mode on an AC input pin, the test receiver output shall be forced to a known initial value on the falling edge of TCK in the Capture-DR TAP controller state, and this initial value shall be retained as long as there is not a different valid logic level on the pin, as described in rule b) above, during the period from the fall of TCK to the rise of TCK in the Capture-DR TAP controller state.

e) Whenever a test receiver is operating in the level-detection mode on an AC input pin and there is a valid logic level on the pin as described in rule b) above that remains or becomes valid for a minimum duration of T_{hyst} after the fall of TCK in the Capture-DR TAP controller state, the test receiver output shall assume the value corresponding to the most recent valid input level and that value shall be retained until the rising edge of TCK in the Capture-DR TAP controller state

f) Whenever a test receiver is operating in level-detection mode on an AC input pin, the output of the test receiver shall be captured in the capture latch of the Boundary-Scan register cell associated with the pin at the rising edge of TCK in the Capture-DR TAP controller state.

6.2.2.2 Permissions

a) Per rules 6.2.2.1d) through f), the output of the test receiver is only relevant during the window of time between the falling and rising edges of TCK in the Capture-DR TAP controller state, and this output may be considered a “don’t care” at other times.

6.2.2.3 Recommendations

a) The amount of hysteresis delay T_{Hyst} should be chosen by the designer to reject common noise sources such as ringing or over/undershoot that may occur on a signal pin.

6.2.2.4 Description

In level-detection mode, the test receiver is a fixed-threshold single-ended logic comparator with hysteresis. Per rule 6.2.2.1a), the designer defines the parameters of this comparator. Because of this single-ended fixed-threshold nature, it is possible that a test receiver in level-detection mode will not be able to discern both logic states produced by an upstream driver when they are DC coupled. This can happen when a driver from a dissimilar logic family is DC coupled to a receiver, or when a shorting defect in an AC coupled structure creates a DC coupling. (The edge-detection mode, described in section 6.2.3, overcomes this problem.)

Rule 6.2.2.1b) defines a *valid logic level* as a signal persisting at one logic level at least a hysteresis level beyond the threshold for a minimum period of time. The IC designer may choose a threshold value at the midpoint of a voltage swing deemed optimal for the mission receiver. This may be the same voltage used to bias the mission receiver when it is AC coupled as seen in Figure 12 (page 18). The hysteresis voltage (V_{Hyst_Level}) will eliminate response to small-amplitude noise. The hysteresis delay period (T_{Hyst}) will eliminate response to short-duration large-amplitude pulses. For example, if the hysteresis delay is set to 5 times the value of T_{Trans}, this will allow the receiver to ignore typical ringing that may occur on transitions or due to other coupled noise. The designer should contemplate the nature of noise sources that may impact signals received at a pin when choosing the hysteresis delay. (See section 4.11.)

Rules 6.2.2.1d) and e) define the behavior of the hysteretic memory of this level detection. If during the time between the falling edge of TCK and the capture of data at the rising edge of TCK in the Capture-DR TAP controller state there is a valid level, this level is captured. If the level is not valid, then a default initial value is captured (see Figure 38). This determines the result when an AC coupled signal decays to an invalid level before the sample interval. The time between the falling and rising edges of TCK in the Capture-DR TAP controller state is a window of input observation and of vulnerability to noise events with magnitude sufficient to disturb the validity of the level appearing on the pin. See Figure 31 (page 33) for an example of one way to implement the (DC) EXTEST capability.

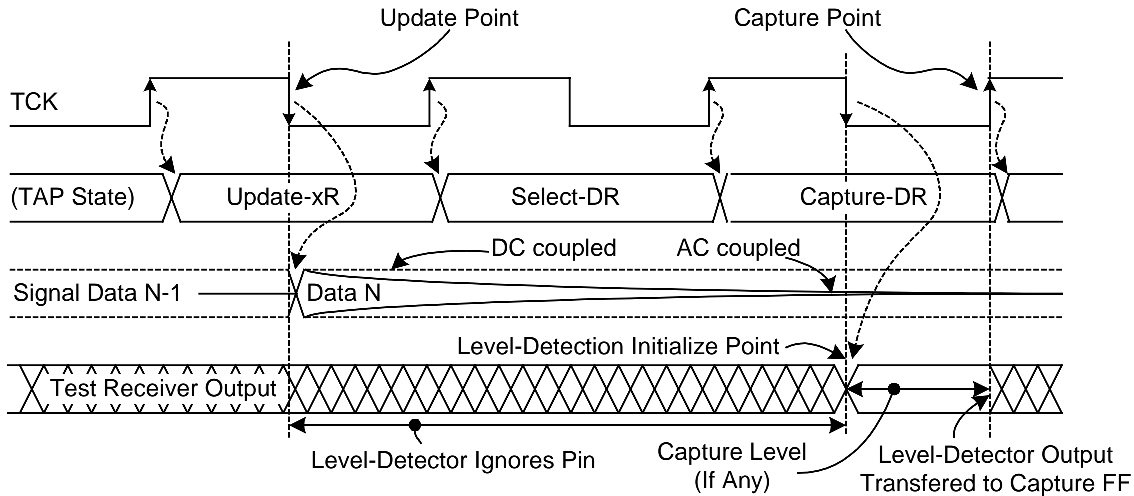


Figure 38: Timing of level-detection initialization and data capture in a test receiver.

6.2.3 Edge Detection Behavior of Input Test Receivers

The edge detection behavior is selected by an AC testing instruction, either EXTEST_PULSE or EXTEST_TRAIN, provided by this standard.

6.2.3.1 Rules

a) Whenever a test receiver is operating in edge-detection mode on an AC input pin, it shall determine the magnitude of input signal change by one of two methods:

i. by comparing the instantaneous voltage on the pin to the recent average of the voltage on the pin, determined by a method equivalent to that given in recommendation 6.2.3.2b), or

ii. if a device input *is guaranteed* to be AC coupled to its driver, by comparing the instantaneous voltage on the pin to a fixed threshold voltage.

NOTE 1 – Even when method ii is permitted, method i may still be exercised.

NOTE 2 – The opportunity to implement method ii clearly exists in the case where the AC coupling is implemented on-chip. It may also apply to a device not containing AC coupling when the device designer assures that in all applications the input will be AC coupled at the board or system level.

NOTE 3 – When adopting method ii, the device designer may choose a threshold value at the midpoint of a voltage swing deemed optimal for the mission receiver. This may be the same voltage used to bias the mission receiver when it is AC coupled as seen in Figure 12 (page 18).

NOTE 4 – If method ii is adopted, then rule b) below must be interpreted as defining hysteresis centered at the fixed threshold voltage.

b) Whenever a test receiver is operating in edge-detection mode on an AC test input pin, the test receiver shall respond only to transitions having a magnitude greater than the hysteresis voltage V_{Hyst_Edge}, where V_{Hyst_Edge} is a fraction no less than 50% of ΔV_{Min} and no greater than 90% of ΔV_{Min}.

NOTE – See rules d) and e) below for further definition of the meaning of the word “respond.”

c) Whenever a test receiver is operating in edge-detection mode on an AC input pin, the test receiver shall respond to valid signal transitions defined in rule 6.2.1.1b) only when the new signal level persists for at least a minimum period of time called the *hysteresis delay*

(T_{Hyst}) and this delay period shall be chosen by the designer by considering recommendation 6.2.2.3a).

NOTE – There may also be a propagation delay in the test receiver. This time is not included in the value of the hysteresis delay. This delay should be small compared to the value of T_{LP} given in rule g) below.

d) In response to a valid signal transition as defined in rules b) and c) above, the test receiver shall output a logic one when the signal transition is rising or a logic zero when the signal transition is falling, and it shall retain that logic value until the next valid transition occurs.

e) If a test receiver has not received a valid signal transition as defined in rules b) and c) above, it shall produce a default output of either a logic one or logic zero.

f) When an AC input pin is AC coupled to a driver, the time constant (T_{HP}) of the effective high-pass filtering of the coupling shall be no less than HP_Mult times the value of the hysteresis delay T_{Hyst}, where HP_Mult is chosen per rule i) below.

g) When method i of rule a) above has been exercised, the time constant (T_{LP}) of the low-pass filter given in recommendation 6.2.3.2b) shall be no less than *LP_Mult* times the value of the hysteresis delay T_{Hyst}, where LP_Mult is chosen via rule i) below.

NOTE – When method ii rather than method i of rule a) is exercised, this rule is unnecessary since recent signal history is not used as a reference.

h) When rules f) and g) above have been exercised, the value of T_{HP} shall be no less than HPLP_Ratio times the value of T_{LP}, where HPLP_Ratio is chosen from Table 3 (page 53).

i) The choice of HP_Mult and (if needed) LP_Mult are found by selecting values from Table 4 (page 53) for the value of V_{Hyst_Edge} closest to or higher than the value used in the design.

NOTE – No value of LP_Mult is needed when method ii rather than method i of rule a) is exercised.

j) When method i of rule a) above has been exercised, tools that perform tests shall assure, when an AC testing instruction is in effect in any IC participating in those tests, that the time between subsequent test data changes (T_{Test}) is no less than 3 (three) times the low-pass filter time constant (T_{LP}) of any IC.

NOTE – When method ii rather than method i of rule a) is exercised, this rule is unnecessary since recent signal history is not used as a reference.

6.2.3.2 Recommendations

a) For better small-amplitude noise immunity, the value of V_{Hyst_Edge} selected per rule 6.2.3.1b) should be set closer to the high limit.

NOTE –Proper accounting for process variations that may affect the value of this threshold should be observed to stay within the limits given in rule 6.2.3.1b).

b) The “recent average” of a signal may be generated with a simple low-pass filter.

NOTE 1 – See Figure 28 (page 30) for an example of this filter.

NOTE 2 – See rule 6.2.3.1g) above for the time constant determination for this low-pass filter.

6.2.3.3 Description

Rule 6.2.3.1a) specifies two methods for detecting edges, the first by comparing the instantaneous value of the signal against its recent history. See Figure 28 (page 30) for an example of one way to do this comparison. The second method allows the comparison to be done versus a fixed reference, when the signal is guaranteed to be AC coupled. This can be the case where the coupling is integrated into the device. A designer is not required to use this second method, but

may find it useful to reuse a portion of the circuitry needed for level-detection (see rule 6.2.2.1a)). In such cases, the values of V_{Hyst_Level} and V_{Hyst_Edge} may be equivalent.

Rule 6.2.3.1b) defines the range for the hysteresis voltage V_{Hyst_Edge} between 50% and 90% as the target for a designer to set a trip point value for test receiver response and allows for significant margin. See recommendation 6.2.3.2a). See also rule 6.2.3.1i), which uses this value to determine bounds on time constants.

Rule 6.2.3.1c) defines the hysteresis delay T_{Hyst} used to provide noise rejection. If a signal change does not persist long enough (for example, it is a short noise pulse) the hysteresis delay will suppress the test receiver's response to it. This gives the test receiver two methods for ignoring noise. The hysteresis voltage will ignore small-amplitude noise and the hysteresis delay will ignore large-amplitude pulses of insufficient duration. See section 6.2.3.4 for a discussion of how hysteresis delay may be controlled within an implementation.

Rule 6.2.3.1g) governs the low-pass time constant (or equivalent) that is used to establish the recent average value of a signal. The low-pass filter time constant is set large enough to assure that the recent history of the average input voltage is not unduly influenced by the rise time of the signal itself and small enough to settle before a new test-induced transition arrives.

Rules 6.2.3.1d) and e) specify the behavior of the test receiver when transitions occur or do not occur. When no transitions have been received, the hysteretic memory of the test receiver will retain a default initial value.

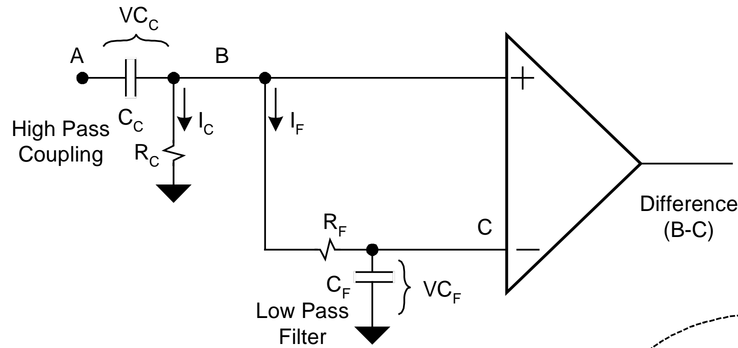
Rule 6.2.3.1f) specifies the minimum value for the high-pass time constant when AC coupling is used. An upstream driver is expected to produce edges that are equal to or faster than the minimum input swing ΔV_{Min} within a maximum time T_{Trans}, given an acceptable level of AC attenuation in the channel. These edges will pass through this high-pass coupling virtually unchanged. This rule assures the subsequent decay will be much slower than a valid signal edge so it will not be confused with a valid signal transition, as depicted in Figure 36 (page 42).

When the high-pass AC coupling is implemented on a board rather than inside an IC, the IC designer shall communicate to the board designer this minimum time constant required for AC coupling. In a 50 ohm load termination environment, the minimum value of capacitance specified by this rule might be 1000 picofarads. If the same time constant were implemented on-chip, then the resistive component would likely be determined by a biasing network and the capacitance could be much smaller, for example 10 Kohms and 5 picofarads, which are both amenable to on-chip integration.

In rule 6.2.3.1g), the value of HPLP_Ratio is a function of the ratio of the minimum input swing from rule 6.2.1.1b) to the maximum input swing from rule 6.2.1.1c), times the V_{Hyst_Edge} fraction. Values of HPLP_Ratio closer to one (1) yield poorer noise immunity. Ratios much larger than one (1) have higher value for noise immunity but force larger values of resistor/capacitor combinations in the coupling network.

Rule 6.2.3.1j) governs the behavior of tools that perform tests, assuring that transitions caused by a tool do not occur too close together in time. This rule assures that the recent history of a signal is not influenced by the recent history of the test.

Given a model of the basic test receiver circuit that uses high-pass coupling and low-pass filtering to generate a self-referenced edge detector (one half shown in Figure 39) the effects of the rules given in section 6.2.3 are plotted in Figure 40 for a single rising edge transition.



Voltage at A: VA = Input Stimulus

Voltage at B: $VB = VA - VC_C$

Current through R_C: $I_C = VB / R_C$

Current through R_F: $I_F = (VB - VC_F) / R_F$

Voltage across C_C: $VC_C = (I_C + I_F) * \Delta t / C_C + VC_C$

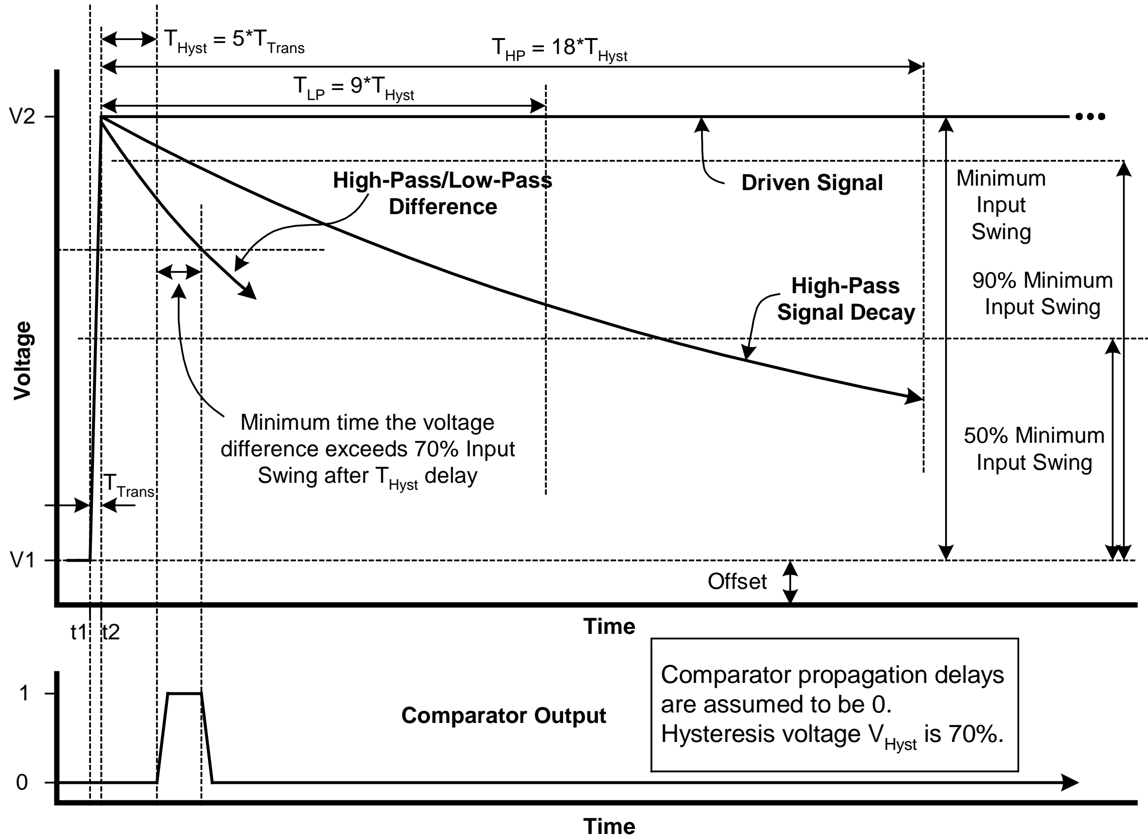
Voltage across C_F: $VC_F = I_F * \Delta t / C_F + VC_F$

Time t+1 Time t

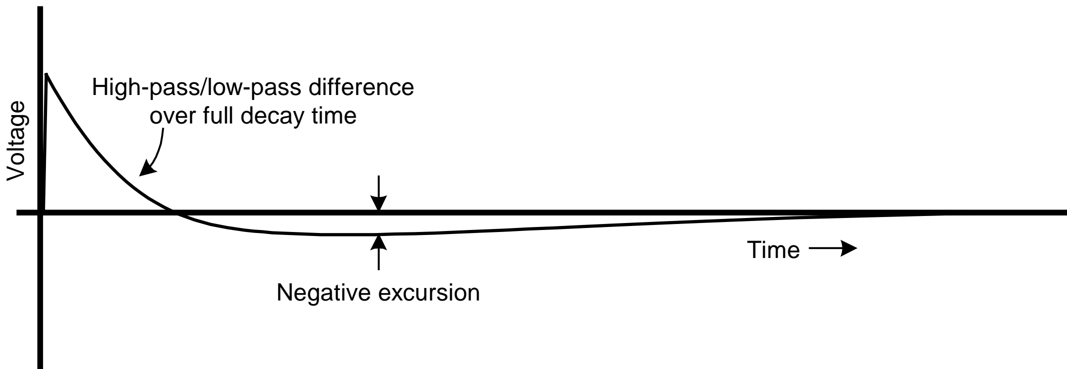
Figure 39: Model with recurrence equations for a portion of test receiver circuitry. The comparator has hysteresis delay. The hysteresis voltage has been omitted in this figure and subsequent analysis.

Figure 40 shows the output of the non-hysteretic comparator in Figure 39 to illustrate the effects of the selected time constants and offsets for a single rising edge, on that portion of circuitry devoted to detecting a rising edge. Rule 6.2.3.1b) gives the two horizontal lines for 50% and 90% input voltage swings. This example uses hysteresis voltage V_{Hyst_Edge} at 70% of the minimum input swing. Given a signal with a valid rising edge with rise time T_{Trans} the output of the high-pass filter will decay as shown. There must be, by rule 6.2.3.1c), a hysteresis delay T_{Hyst} where the comparator does not respond. The time constant T_{HP} of decay due to the high-pass filter, by rule 6.2.3.1f) must be no less than 18 times (in this example) the value of T_{Hyst}. However, the decay of the difference signal is faster as shown, due to the low pass filtering set to no less than 9 times the value of T_{Hyst} by rule 6.2.3.1g). The choice of multipliers (9 and 18, from Table 4) assure that the minimum time that the voltage difference exceeds 70% of the minimum input swing is significantly greater than the hysteresis delay. If the either or both multipliers are increased, this minimum time will increase. If the hysteresis voltage is decreased from 70%, the minimum time will increase. Finally, if the circuit is DC coupled (equivalent to an infinite coupling time constant) the minimum time will increase.

Rule 6.2.3.1h) controls the ratio of high-pass to low-pass time constants via the content of Table 3 below. The ratio is selected by first determining the ratio of driven signals the receiver is prepared to accept, $\Delta V_{Min} / \Delta V_{Max}$ and using this ratio to de-rate V_{Hyst_Edge}. The comparator takes the difference of the high-pass filtered and low-pass filtered signals, and after much of the transition effect has decayed, this difference can drop below zero. (This is seen in Figure 41, which depicts a complete transition and decay cycle.) When a larger signal is applied, this multiplies the negative excursion. In order to prevent this negative excursion from re-triggering the test receiver in the negative direction, the high-pass and low-pass time constants are adjusted to prevent this. As the ratio of these two constants gets larger, the negative excursion is reduced. In the extreme case of an infinite ratio (DC coupling) there is no negative excursion.



1 **Figure 40: Relationships of key delay times and time constants given by rules in section 6.2.3.1 for the**
2 **detection of a rising edge. Here the value of V_{Hyst} has been set to 70% of the minimum input swing.**



3 **Figure 41: High-pass/low-pass difference signal over the full decay time.**

Table 3: Values of multiplier HPLP_Ratio versus V_{Hyst_Edge} times the voltage ratio ΔV_{Min} over ΔV_{Max}.

V_{Hyst_Edge} * $(\Delta V_{Min}/\Delta V_{Max})$	HPLP_Ratio	Comments
> 0.13	2	12.5% actual over/undershoot (worst case)
Between 0.13 and 0.10	4	9.9%
Between 0.10 and 0.09	6	8.2%
Between 0.09 and 0.07	8	6.9%
Between 0.07 and 0.06	12	5.8%
Between 0.06 and 0.05	16	4.3%
< 0.05	32	2.5%

Rule 6.2.3.1i) selects minimum values for HP_Mult and LP_Mult (from Table 4 below) which determine high-pass and low-pass time constants. This is consistent with rule 6.2.3.1h) which may have the effect of raising HP_Mult above the minimum value.

Table 4: Values of multipliers HP_Mult and LP_Mult for selected values of hysteresis voltage V_{Hyst}.

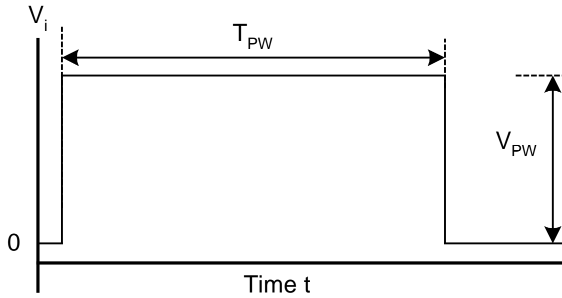
V_{Hyst} % ΔV_{Min}	HP_Mult	LP_Mult	Comments
50%	10	5	Lowest small signal noise immunity for positive noise events. Highest small signal noise immunity for negative noise events. Gives smallest values for on-chip filter components.
60%	12	6	
70%	18	9	Best small signal noise immunity for general noise events.
80%	30	15	
90%	75	37	Highest small signal noise immunity for positive noise events. Lowest small signal noise immunity for negative noise events. Gives highest values for on-chip filter components.

6.2.3.4 Noise Rejection in the Edge-Detecting Mode

The hysteresis delay T_{Hyst} used to provide noise rejection during edge-detection mode. The hysteresis voltage setting will reject a noise pulse with small amplitude. But if a noise pulse with amplitude greater than the hysteresis voltage is encountered, the test receiver is expected to reject those with duration less than T_{Hyst}. There are two techniques that can be utilized separately or in combination to accomplish this. (Other techniques may also be applied to achieve this result.) These techniques are *bandwidth limitation* and *slew rate limitation*.

6.2.3.4.1 Noise Rejection by Bandwidth Limitation

Bandwidth limitation can be added to the test receiver to limit its response time. Consider a rectangular pulse waveform of height V_{PW} and pulse width duration T_{PW}, where V_{PW} is greater than the hysteresis voltage. (See Figure 42.) For analysis purposes, assume that the lower amplitude of the pulse is at 0 volts, although the results are applicable to the general case of an arbitrary baseline voltage. Furthermore, assume the rise and fall times of the pulse are much faster than the those of the test receiver input stage so they can be ignored in this analysis, but the test receiver input stage is adequately fast enough to track the pulse itself.



1 **Figure 42: Pulse input to test receiver.**

2 The test receiver can be modeled in the small-signal domain as a single-pole low-pass amplifier
3 with a frequency response (as designated by the lowercase nomenclature) given in Equation 1
4 where v_o and v_i are the output and input voltages of the amplifier and A_0 is its DC gain. Let
5 $\tau_{BW} = 1/2\pi f_{BW}$ be the time constant of the bandwidth frequency, f_{BW} and s be the complex identity
6 jω.

$$\frac{v_o}{v_i} = \frac{A_o}{1 + s\tau_{BW}}$$

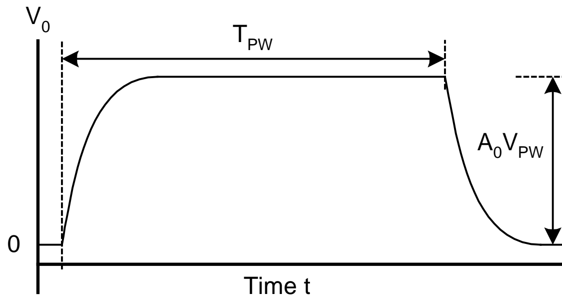
7 **Equation 1: Frequency response of a simple single-pole low-pass amplifier.**

8 Furthermore, assume that the test receiver has an input referred switching threshold of V_{TH}. The
9 input voltage must exceed V_{TH} for a sufficient period of time to cause the test receiver to switch
10 its output state. In the time domain (as designated by the upper case nomenclature) the output
11 response of the test receiver will be described by Equation 2 which is shown in Figure 43 for
12 $T_{PW} >> \tau_{BW}$.

13 NOTE – The propagation delay through the test receiver has been ignored.

$$\frac{V_o}{V_i} = A_o\left(1 - \exp(-t/\tau_{BW})\right)$$

14 **Equation 2: Time domain output response of the test receiver.**



15 **Figure 43: Output response of the test receiver to the rectangular pulse.**

16 The output amplitude for an arbitrary input can be obtained by solving Equation 2 as

$$t = -\tau_{BW} \ln\left\{1 - \left(\frac{V_o}{ViA_o}\right)\right\}.$$

17 **Equation 3: Solution of Equation 2 for time t.**

18 In order to for the receiver circuitry to switch the input amplitude will have to exceed the input
19 referred switching threshold for a period of time long enough to allow the output level to reach

the output referred switching threshold, A_oV_{TH}. Thus, the input pulse must persist for a minimum period of time, T_{TH}. This time can be calculated from Equation 3 as

$$T_{TH} = -\tau_{BW} \ln\left\{1 - \left(\frac{V_{TH}}{V_{PW}}\right)\right\}$$

Equation 4: Minimum pulse width duration.

If the pulse width is less than the minimum time, T_{TH}, then the pulse will be rejected. Alternately, the pulse will be rejected if the bandwidth of the receiver circuit is

$$f_{BW} < -\frac{1}{2\pi T_{PW}} \ln\left\{1 - \left(\frac{V_{TH}}{V_{PW}}\right)\right\}$$

Equation 5: Test receiver bandwidth specification.

6.2.3.4.2 Noise Rejection by Slew Rate Limitation

In most situations the switching of the test receiver will be limited more by its large signal and internal slew capability rather than its small signal bandwidth. This is manifested by the limited rate at which an arbitrary internal node of the receiver can transition due to its capacitive load and/or limited current drive capability. Hence, at this internal node of the test receiver circuitry, the voltage V_{INT} will be limited by its slew rate SR, as depicted in Figure 44.

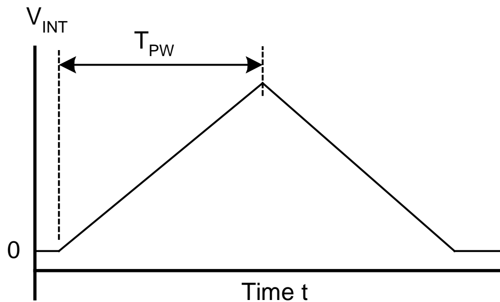


Figure 44: Slew rate limited response of a control node internal to the test receiver.

It is assumed that the duration of the input signal is not long enough to allow the internal node voltage to achieve its final value for the given level of input signal before the direction of the voltage transition reverses as the result of the reversal of the input signal. In order for the circuit to switch the voltage at the internal node, it will have to achieve a level equal to its internal switching threshold V_{THINT}. This situation can be expressed as the switching condition

$$V_{INT} = SR \bullet T_{PW} > V_{THINT}$$

or

$$T_{PW} > \frac{V_{THINT}}{SR}$$

If the duration of the input pulse does not meet the criteria set forth in this equation, it will be rejected.

6.3 Output Drivers

All AC pins (see 4.1) that drive data from an IC are equipped with test circuitry that allows Boundary-Scan test instructions to co-opt the mission driver and substitute a time-varying signal

in place of mission data. The goal is to use the mission driver with its *native drive levels* and *edge rate* to produce test signals (as defined in section 6.2). This is conceptualized in Figure 45 for a differential mission driver, but the concept is identical for single-ended drivers.

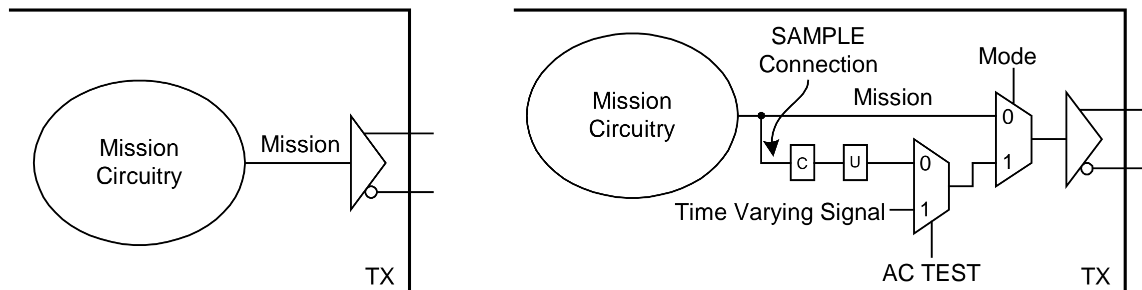


Figure 45: A mission driver (differential) and added test circuitry.

The actual implementation may be different, since adding a multiplexer (as shown) in the mission signal path may introduce an unacceptable delay, but the effect is the same as shown. The test circuitry used to implement the functionality is not required to perform at the frequencies of the mission, except with respect to voltage levels and edge rates seen at the pin(s). The time between test edges will likely be much larger than for mission edges.

The mission circuitry may be digital or analog. If digital, it could operate at extremely high frequencies so as to have ‘analog’ properties. In many cases, the signal states captured via the ‘SAMPLE connection’ to the Boundary-Scan capture flip-flop may be indeterminate. This is especially true in cases where the TCK rate is much lower than the performance of the mission circuitry. Thus this standard allows the relaxation of the requirement from IEEE 1149.1 to implement the SAMPLE instruction for AC output pins – the SAMPLE instruction must be implemented, but the SAMPLE connection shown may be omitted and replaced with a default value. If the mission of the device *is* a candidate for use with the SAMPLE instruction, then SAMPLE functionality should be implemented.

NOTE – The SAMPLE instruction must be implemented on DC pins and all inputs.

6.3.1 AC Pin Driver Behavior for IEEE Std 1149.1 Test Instructions

Test mode instructions from IEEE Std 1149.1 include EXTEST and CLAMP, and within options contained within IEEE Std 1149.1, the RUNBIST and INTEST instructions may also provide data to the driver, when they do not disable all drivers. The HIGHZ instruction always disables drivers. The rules below assume there is an appropriate load or termination available to allow a driver to operate as specified for its mission mode when enabled.

Non-test mode instructions (e.g., SAMPLE, PRELOAD, BYPASS, IDCODE, USERCODE) do not interfere with the mission performance of the driver.

6.3.1.1 Rules

a) The single-ended or differential driver for an AC output pin or channel shall be provided with data by a single associated Boundary-Scan register cell.

b) When performing EXTEST, an enabled output driver of a single-ended AC output pin shall produce on its output a static value that matches the value stored in the Update flip-flop of the associated Boundary-Scan register cell.

NOTE – Depending on if permission 6.3.1.2a) is implemented, an output driver may always be enabled.

c) When in test mode, an enabled output driver of a differential AC output channel shall produce on its positive leg pin a static value that matches the value stored in the Update

flip-flop of the associated Boundary-Scan register cell, and the opposite value on its negative leg pin.

d) When in test mode, an enabled output driver of an AC output pin (channel) shall produce on its output(s) a transition matching the levels and edge rate of the mission performance specified for the driver, when the content of the Update flip-flop of the associated Boundary-Scan register cell changes.

e) When in test mode, a disabled output driver of an AC output pin (channel) shall produce on its output(s) a quiescent, non-driven state.

NOTE 1 – There may be biasing supplied in the driver implementation that establishes a state as perceived by a downstream receiver, but this state is at most weakly driven. It is expected that if another enabled driver shared this channel, it would be unaffected by this weak state.

NOTE 2 – A driver may be disabled (see permission 6.3.1.2a)) by a control cell, or by an instruction such as RUNBIST, INTEST or HIGHZ.

6.3.1.2 Permissions

a) The single-ended or differential driver for an AC output pin (or channel) may be disabled or enabled via the content of a control cell in the Boundary-Scan register, per the rules within IEEE Std 1149.1.

b) With respect to the SAMPLE instruction, the device designer may choose to have the Capture flip-flop load a deterministic value rather than attempt to sample the state of the mission circuitry on the rising edge of TCK in the Capture-DR TAP controller state.

c) Observe-only Boundary Register cells may be connected to AC output pin(s) to observe the driven state of the pin(s).

NOTE – Additional observe-only cells are also allowed by IEEE Std 1149.1-2001, see section 11.8, “Redundant cells”. Here they are explicitly allowed on negative as well as positive legs of differential AC channels.

d) The state of a single-ended AC output pin or the positive leg pin of a differential AC channel may be captured by the data cell for that pin while the EXTEST, EXTEST_PULSE or EXTEST_TRAIN instructions are loaded.

NOTE – This allows a driver to “self monitor” its ability to create a logic state on its pin by using the capture stage of it Boundary Register data cell. This concept also comes from IEEE 1149.1-2001, section 11.6, “Provisions and operation of cells at system logic outputs”.

6.3.1.3 Recommendations

a) When the mission circuitry is digital, or is capable of slower digital performance, the designer should implement the SAMPLE instruction behavior per IEEE Std 1149.1.

6.3.1.4 Description

For AC pins only, permission 6.3.1.2b) allows a device designer to opt out of the requirement by IEEE Std 1149.1 that mandates capturing the digital state of the mission circuitry on the rising edge of TCK in the Capture-DR TAP controller state while executing the SAMPLE instruction, since there are cases where this signal is analog in nature, or if digital, it is changing so quickly as to make sampling at the much slower TCK rate meaningless. If, when SAMPLE is loaded, the mission can be suitably observed (e.g. there is a single-cycle mode) then the designer should implement SAMPLE as recommended in 6.3.1.3a).

Permissions 6.3.1.2c) and d) allow a designer to add output pin monitoring capacity, useful in determining if a driver can successfully achieve a logic state on its pin(s). This is useful for finding shorted driver pins. Permission 6.3.1.2c) does this with additional, redundant cells. Permission d) does this with the capture stage of the associated data cell.

6.3.2 AC Pin Driver Behavior for Test Instructions Provided by This Standard

This standard provides two new instruction, EXTEST_PULSE and EXTEST_TRAIN. These instructions are AC test mode instructions that use the same Boundary-Scan register cells already specified for the IEEE Std 1149.1 instructions, that is, the mapping of data and control cells does not change.

6.3.2.1 Rules

a) The single-ended or differential driver for an AC output pin (or channel) shall be provided with data by a single associated Boundary-Scan register cell, and that cell shall be the same required by rule 6.3.1.1a).

When in AC test mode, an enabled output driver of an AC output pin (channel) shall produce on its output transitions matching the levels and edge rate of the mission performance specified for the driver.

NOTE – Depending on if permission 6.3.1.2a) is implemented, the pin or channel may always be enabled.

c) When in AC test mode, an enabled output driver of an AC output pin (channel) shall produce on its output a transition when the content of the Update flip-flop of the associated Boundary-Scan register cell changes.

d) For single-ended AC pins, when in AC test mode, if AC behavior of this driver is not disabled by an AC/DC selection cell, an enabled output driver of an AC output pin shall produce on its output a state matching the content of the Update flip-flop of the associated Boundary-Scan register cell when AC Test Signal is de-asserted, and the opposite state when AC Test Signal is asserted.

NOTE 1 – See section 6.5 for information on AC/DC selection cells.

NOTE 2 – If no AC/DC selection cell is present for this driver, it is always enabled for AC behavior when in AC test mode.

NOTE 3 – The AC Test Signal is generated by the EXTEST_PULSE and EXTEST_TRAIN instructions (see sections 5.3 and 5.4).

e) For differential AC pins, when in AC test mode, if AC behavior of this driver is not disabled by an AC/DC selection cell, an enabled output driver of an AC output channel shall produce on its positive leg output a state matching the content of the Update flip-flop of the associated Boundary-Scan register cell when AC Test Signal is de-asserted, and the opposite state when AC Test Signal is asserted, and its negative leg shall produce the opposite values.

f) When in AC test mode, a disabled output driver of an AC output pin (channel) shall produce on its output(s) a quiescent, non-driven state.

NOTE 1 – There may be biasing supplied in the driver implementation that establishes a state as perceived by a downstream receiver, but this state is at most weakly driven. It is expected that if another enabled driver shared this channel, it would be unaffected by this weak state.

NOTE 2 – A driver may be disabled (see permission 6.3.1.2a)) by a control cell.

6.3.2.2 Description

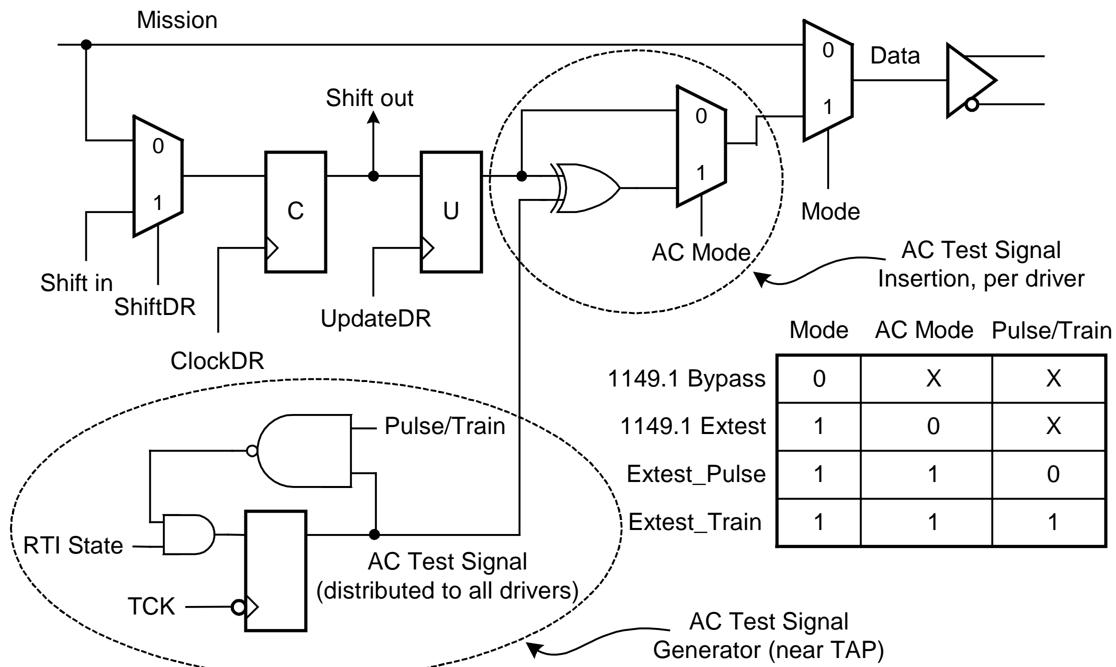
When either the EXTEST_PULSE or EXTEST_TRAIN instruction is in effect, an enabled AC pin driver will produce an AC waveform (or its complement on the negative leg of differential pair) with the same voltage range and edge rate that the driver produces in mission mode, when the TAP passes through the *Run-Test/Idle* TAP controller state. This has important implications for any test receiver connected on downstream AC input pins. The test receiver contains a hysteretic memory that is first initialized to a default state. If the test receiver never sees a valid edge, this default state is retained. This can be used to detect open pins. If a driven edge is

received, the hysteretic memory will be set to the logic value the upstream driver even though this value may decay due to AC coupling. The AC Test Signal assures that for any sequence of test data loaded into the Update flip-flop over time, including sequences of like data, there will be transitions generated that pass through the AC coupling for interpretation by the test receivers.

When the TAP does not traverse the *Run-Test/Idle* TAP controller state, the effect of both the EXTEST_PULSE or EXTEST_TRAIN instructions is the same as (DC) EXTEST, because the AC Test Signal remains de-asserted.

6.4 Example AC Pin Driver Structure

A possible implementation for a pin driver is shown in Figure 46 that supports IEEE Std 1149.1 instructions as well as AC test capabilities provided by this document. This implementation is a simple adaptation of a commonly used Boundary-Scan register cell design (BC_1), where an extra multiplexer, controlled by "AC Mode" is used to select either the Update register content, or that same content modulated by an exclusive-OR gate with the AC Test Signal. Other cell designs from IEEE Std 1149.1 can be modified in similar fashion.



	Mode	AC Mode	Pulse/Train
1149.1 Bypass	0	X	X
1149.1 Extest	1	0	X
Extest_Pulse	1	1	0
Extest_Train	1	1	1

Figure 46: A general AC pin driver structure.

6.5 AC/DC Selection Cells

There may be cases during the execution of tests where the ability to disable the AC signal appearing on an AC pin driver may be desirable when the device is executing either the EXTEST_PULSE or EXTEST_TRAIN instructions. When the AC signal is disabled, the DC behavior of that driver is reinstated, as if the EXTEST instruction were operating. This allows fixed logic levels to be maintained on selected drivers while others are in AC mode.

This necessitates a controlling structure, and this standard adopts a structure much like the driver enable/disable capability allowed by IEEE Std 1149.1. That capability is implemented by "control cells", which are Boundary Scan register cells that are imposed between the driver enable/disable control lines coming from the mission circuitry and the driver enable, as shown in Figure 47.

NOTE – This standard also allows this exact mechanism for completely disabling a controlled driver (see permission 6.3.1.2a)). AC/DC selection cells are in addition to these.

The driver enable control cell monitors and controls the state of the mission driver enable signal. This monitor capability is not needed for an AC/DC selection cell since there is no mission equivalent signal to be observed. The output of the driver enable control cell is used to directly control the driver enable(s) associated with the control cell. Multiple driver enables may be controlled from a single cell when drivers come in logical groups. Driver control cells are not needed for drivers that cannot be disabled (i.e., 2-state drivers).

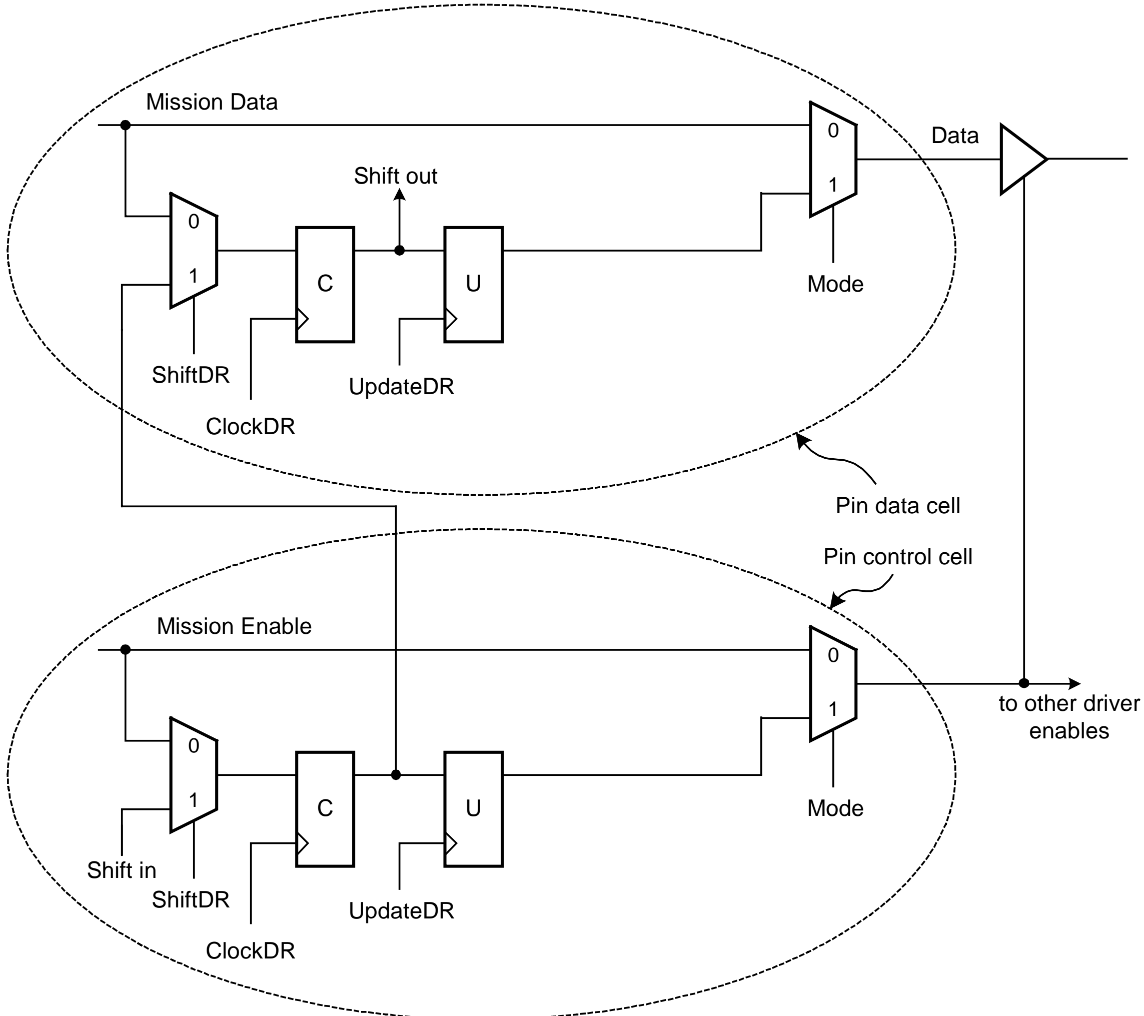


Figure 47: A typical pin driver data and control cell structure from IEEE Std 1149.1.

An AC/DC selection cell modifies the behavior of a data cell, not the driver itself, as shown in Figure 48, for a 2-state driver pin. The AC/DC selection cell simply prevents the modulation of data via the AC Test Signal, for those cells controlled by it. The simple cell as shown does not capture any data, but it is recommended that it capture the output of its Update flip-flop if improved testability of these cells is desired.

Figure 48: An AC pin driver structure with an AC/DC selection cell.

6.5.1 Permissions

a) The device designer may choose whether or not to implement AC/DC selection cells within the Boundary-Scan register, and which and how many AC pin drivers are controlled by these cells, per the rules given in section 6.5.2 below.

b) AC/DC selection cells may be placed in any order within the Boundary-Scan register.

c) AC/DC selection cells may not capture data, or may capture unspecified data, or may capture the content of their Update flip-flops on the rising edge of TCK in the *Capture-DR* TAP controller state, for the SAMPLE, EXTEST, INTEST, EXTEST_PULSE and EXTEST_TRAIN instructions.

6.5.2 Rules

a) If implemented, AC/DC selection cells shall be used to control one or more AC pin drivers.

b) An AC pin driver shall have either zero or one AC/DC selection cells.

c) When an AC/DC selection cell contains a 0, any associated AC pin data cells controlled by it will behave as if EXTEST is being executed when either the EXTEST_PULSE or EXTEST_TRAIN instructions are actually loaded.

NOTE – See section 6.2.3.1 for rules on how AC pin data cells behave as conditioned by AC/DC selection cells.

d) When an AC/DC selection cell contains a 1, any associated AC pin data cells controlled by it will behave as specified for either the EXTEST_PULSE or EXTEST_TRAIN instructions, when these are loaded.

e) AC/DC selection cells shall be composed of a Shift flip-flop and an Update flip-flop, identical to the control cell structure mandated by IEEE Std 1149.1.

f) AC/DC selection cells shall shift data from TDI towards TDO on the rising edge of TCK while in the *Shift-DR* TAP controller state.

g) AC/DC selection cells shall transfer the content of the Shift flip-flop to the Update flip-flop on the falling edge of TCK in the *Update-DR* TAP controller state.

6.5.3 Recommendations

a) AC/DC selection cells should capture the content of the Update flip-flop on the rising edge of TCK in the *Capture-DR* TAP controller state, for the SAMPLE, EXTEST INTEST, EXTEST_PULSE and EXTEST_TRAIN instructions.

NOTE – This may improve the testability of these cells during device manufacture.

b) The quantity of AC/DC selection cells should be minimized to avoid significantly increasing the size of the Boundary-Scan register.

NOTE – This can be accomplished by assigning a single AC/DC selection cell to groups of logically related AC pin drivers.

6.5.4 Description

AC/DC selection cells can be added to a design to allow application software to override AC performance with (DC) EXTEST on selected AC pin drivers. Device designers are given the option to implement these controls on any AC pin drivers of their choosing. Designers of programmable devices may have to implement many of these cells if their devices contain highly flexible I/O pins.

1
2 # 7 Conformance and Documentation Requirements

3 ## 7.1 Conformance

4 ### 7.1.1 Specification

5 Rules

6 a) A component conforming to this standard shall comply with all rules provided herein.

7 NOTE – Due to rule 5.1.1a), this also implies conformance with the rules set out in IEEE Std 1149.1.

8 ### 7.1.2 Description

9 Conformance to the rules set out herein and in IEEE Std 1149.1 are essential for testing boards
10 and other assemblies containing both DC and AC coupled interconnections, allowing
11 manufacturing defects such as shorted or open solder joints to be found and repaired before
12 shipment. Conformance allows:

13 ▪ IC vendors to provide testability features in a standardized way, so that each new IC design
14 does not need new engineering investment to provide testability.

15 ▪ makers of Automatic Test Equipment to develop and continually refine standardized tools for
16 the automation of test development, test execution and diagnosis of failures.

17 ▪ end-users to strategize and develop test methodologies in a standardized way, making full use
18 of the automation provided by tools, to allow them to produce very large and complex boards
19 and system more rapidly and efficiently.

20 ## 7.2 Documentation

21 Because adherence to this standard implies adherence to IEEE Std 1149.1, all ISC devices shall
22 have a description supplied in Boundary-Scan Description Language (BSDL) provided with IEEE
23 Std 1149.1-2001.

24 ### 7.2.1 Specification

25 Rules

26 a) A component conforming to this standard shall be documented with a Boundary-Scan
27 Description Language (BSDL) description.

28 NOTE – See IEEE Std 1149.1-2001 for a description of IEEE BSDL. The precursor to IEEE BSDL
29 developed in 1990 cannot be used for documentation because it does not support the concept of "BSDL
30 Extensions".

31 b) A component shall have both the EXTEST_PULSE and EXTEST_TRAIN instructions
32 and register relationship and optional provisions documented via the syntax provided by
33 BSDL and the BSDL extension provided by this standard.

34 NOTE – New BSDL syntax (contained within a "BSDL extension") for describing concepts and structures
35 introduced by this standard are given in section 7.4. A BSDL extension is a mechanism provided by IEEE
36 Std 1149.1-2001 (see "User extensions to BSDL") which allows proprietary syntax to be provided that will
37 allow tools to work that are unaware of this syntax.

c) Prime and second source devices shall have identical implementations of publicly accessible test circuitry, with the sole exception of the device identification code.

NOTE – This includes Boundary Register cell ordering and analog parameters such as voltage thresholds and time constants.

d) Other properties of a device not described in BSDL shall be documented by the manufacturer.

NOTE – For example, this includes TAP signal voltage level requirements, and any additional power requirements of the device.

7.2.2 Description

Consider a device with a full set of 1149.1 instructions and registers as well as the new AC testing instructions. Here are fragments of BSDL needed to document this device.

First, for devices that have AC differential outputs, a "Port_Grouping" attribute must be given that identifies the positive and negative legs. Notice that because the implementation of AC testing requires single-ended receivers for differential input pin pairs, the test behavior of these pins is single-ended and thus should not be included in a port grouping description. (An error would result during compilation.) For example, for a device with four pairs of differential data drivers, the Port_Grouping could be:

```
Attribute PORT_GROUPING of ACDEV:entity is
  "Differential_Voltage ( "
        "  (D(1), Dbar(1)), "
        "  (D(2), Dbar(2)), "
        "  (D(3), Dbar(3)), "
        "  (D(4), Dbar(4)) )";
```

NOTE 1 – Refer to IEEE Std 1149.1-2001, section B.8.8, titled "Grouped Port Identification", for precise information regarding the Port_Grouping attribute.

NOTE 2 – The entity name in these examples is shown as "ACDEV". This would be replaced with a name unique to the device.

At a board or system level, differential pairs are interconnected with pair-wise wiring or AC blocking capacitors. With the information from the port grouping attribute, software can trace the pathways of the positive and negative legs of each pair starting at the drivers. Thus, though the receivers are not identified as differential, their differential relationship can be discovered via this tracing exercise.

Next, an "Instruction_Opcode" attribute used to define instruction names and binary code assignments should be given:

```
Attribute INSTRUCTION_OPCODE of ACDEV:entity is
  "BYPASS              (111111), " &
  "EXTEST              (000000), " &
  "SAMPLE              (000001), " &
  "IDCODE              (010001), " &
  "USERCODE            (010010), " &
  "EXTEST_TRAIN        (010011), " &
  "EXTEST_PULSE        (000010)  ";
```

NOTE – Refer to IEEE Std 1149.1-2001, section B.8.11, titled "Instruction Register Description", for precise information regarding the Instruction_Opcode attribute.

Later, a Register_Access attribute is given:

```
Attribute REGISTER_ACCESS of ACDEV:entity is
  "Boundary      (EXTEST_PULSE, EXTEST_TRAIN)";
```

The Register_Access attribute defines the existence of optional registers, their length, the instruction(s) that target them, and any consistent capture data they may be loaded with in the *Capture-DR* TAP Controller state. The above attribute documents the fact that AC testing targets the Boundary Register.

NOTE 1 – Refer to IEEE Std 1149.1-2001, section B.8.13, titled "Register Access Description", for precise information regarding the Register_Access attribute.

NOTE 2 – This attribute may also (though redundantly) document the associations of EXTEST, SAMPLE, BYPASS, USERCODE and IDCODE as well. This was omitted here.

7.3 BSDL Extention for Advanced I/O Description (STD_1149_6_200x)

The information provided above in 7.2 showed how to document features of a device implementing AC testing instruction using the existing syntax of BSDL. This information is incomplete. BSDL has been defined (see IEEE Std 1149.1-2001) to be extensible using a mechanism called a "BSDL Extension". A BSDL Extension for describing additional features of advanced I/O devices is given here.

NOTE – Refer to IEEE Std 1149.1-2001, section B.8.17, titled "User extensions to BSDL", for precise information regarding BSDL extensions.

The extension mechanism chosen for describing devices is based on the definition of a VHDL package with the name "STD_1149_6_200x" which contains the definitions of attributes that will be used to supply relevant data. Therefore, a compliant device BSDL will contain an additional "use" statement appearing just after the "standard use statement" as in this excerpt of a BSDL file:

```
  …
use STD_1149_1_2001.all;    -- Standard 'use' statement
use STD_1149_6_200x.all;      -- BSDL Extension for AIO
  …
```

NOTE – Refer to IEEE Std 1149.1-2001, section B.8.5, titled "Use Statement", for precise information regarding references to additional packages.

Utilization of the extension mechanism of BSDL guarantees that advanced I/O information can be supplied to applications that are cognizant of this functionality without hindering other applications that may not be aware of this functionality. Non-cognizant applications will simply ignore the extension.

BSDL extensions may also be used to define new Boundary-Scan register cell types. This standard creates two new cell types to describe the cell behavior of AC/DC selection cells as defined in section 6.5. The simplest cell is mandated by permission 6.5.1c), which allows the cell to capture nothing, or unspecified data ('X'). Recommendation 6.5.3a) advises the capture of the Update flip-flop content. In either case, this is true for the SAMPLE, EXTEST INTEST, EXTEST_PULSE and EXTEST_TRAIN instructions. The BSDL language allows cell constant information to describe cell capture information for the SAMPLE, EXTEST and INTEST instructions defined by IEEE 1149.1. It does not allow new instructions (i.e., EXTEST_PULSE and EXTEST_TRAIN) to be used as instruction names. Rather than change the BSDL language to allow these new instructions, and because there is no difference in capture behavior allowed for any instruction by this standard, this standard adopts the convention that the EXTEST instruction

name is representative of both DC EXTEST and the two AC test instructions provided by this standard. Thus in the cell definitions given below, only EXTEST will be listed, but it implies all three, EXTEST, EXTEST_PULSE and EXTEST_TRAIN instructions.

The cell context (see IEEE Std 1149.1-2001, section B.10.2.1, “Cell context values”) for AC/DC selection cells is, by convention set herein, “Internal”. Since the cell definitions given below do not support any other cell context, an attempt to use another context (e.g., CONTROL) will cause a BSDL semantic error and be rejected. This keeps common tools that are cognizant only of IEEE Std 1149.1 from associating a control capability (used to disable drivers) with AC/DC selection cells. Such software will ignore these cells, except to assure they are always loaded with the specified “safe values” (see IEEE Std 1149.1, section B.8.14.1.4, “The <safe bit> element”).

The VHDL package STD_1149_6_200x contains the definition of additional attributes used to complete the description of the ISC features of a device. The content of this VHDL package is given here.

Syntax

```
Package STD_1149_6_200x is  -- Attribute definitions for AIO
  use STD_1149_1_2001.all;  -- Refer to BSDL definitions

  constant AIO_SelX : Cell_Info;   -- AC/DC selection X
  constant AIO_SelU : Cell_Info;   -- AC/DC selection U

  attribute AIO_Pin_Behavior:   BSDL_Extension;
end STD_1149_6_200x;

Package Body STD_1149_6_200x is
  use STD_1149_1_2001.all;  -- Refer to BSDL definitions

  constant AIO_SelX : Cell_Info:=   -- Captures 'X', unknown data
   ((INTERNAL, SAMPLE, X),
    (INTERNAL, INTEST, X),
    (INTERNAL, EXTEST, X));    -- EXTEST, EXTEST_PULSE, EXTEST_TRAIN

  constant AIO_SelU : Cell_Info:=   -- Captures 'UPD', the Update FF
   ((INTERNAL, SAMPLE, UPD),
    (INTERNAL, INTEST, UPD),
    (INTERNAL, EXTEST, UPD));  -- EXTEST, EXTEST_PULSE, EXTEST_TRAIN
end STD_1149_6_200x;
```

This VHDL package is “read-only” and may be maintained within a given system in the same location as the standard package STD_1149_1_2001.

7.4 BSDL Extension Structure

The following sections define the syntax and applicable semantics for the BSDL attributes defined by the Advanced I/O extension. The form of the syntax used is defined in IEEE Std 1149.1-2001.

NOTE 1 – See IEEE Std 1149.1-2001, “Lexical elements of BSDL” and “Notes on syntax definitions” for the conventions used herein to describe the parsing requirements for BSDL.

NOTE 2 – Syntactic items are shown surrounded in “< >” brackets when referenced in this text. Some of these items will be defined here, and some will be adopted from IEEE Std 1149.1-2001. Those that are adopted will be underlined to indicate their source.

1 When an Advanced I/O extension exists in the extension area of a BSDL description, it must have
2 the structure shown here. The various attributes, both mandatory and optional must appear in a
3 prescribed order and not be intermixed with other statements.

4 NOTE – These other statements include BSDL attributes, attributes for other BSDL extensions and general
5 VHDL constructs.

6 7.4.1 Specification

7 *7.4.1.1 Syntax*

```
8     <AIO Extension> ::=
9       <AIO pin behavior description>                    (see 7.5.1)
```

Editor's Note: At this time there is only one item defined in the BSDL extension. It could expand in the future.

10 *7.4.1.2 Rules*

11 a) The syntax for an <AIO Extension> as it appears in the extension area of a BSDL
12 description shall be that shown above.

13 NOTE – The attributes must appear in the order shown above.

14 *7.4.1.3 Permissions*

15 a) An <AIO Extension> may appear anywhere in the extension area of a BSDL description,
16 subject to any rules defined by other extensions as to ordering.

17 NOTE – If more than one extension exists, an <AIO Extension> may appear before or after any of them
18 within the limits of their definitions.

19 7.4.2 Description

20 At this time there is only one element within an <AIO Extension>. No other statements may be
21 intermixed within the extension, as the syntax described herein specifies. This extension may
22 coexist with, either preceding or following other extensions.

23 7.4.3 Keywords for Advanced I/O BSDL

24 This subsection lists the keywords of Advanced I/O BSDL. These keywords are in addition to the
25 reserved words of BSDL and VHDL. (See "BSDL reserved words" and "VHDL reserved and
26 predefined words" in IEEE Std 1149.1-2001.)

27 **AIO_Pin_Behavior**

28 *7.5 BSDL Attribute Definitions*

29 The mandatory and optional attributes needed to describe the ISC properties of a device are given
30 in the remainder of this section. They must appear in the order given in 7.4.1.

31 7.5.1 Attribute AIO_Pin_Behavior

32 The mandatory AIO_Pin_Behavior attribute is used to enumerate those system pins of a
33 component that are "AC" pins per rule 6.1.1a), and have been provided with Advanced I/O
34 capability. The description may also include information about any AC/DC control cells for these

pins, and what the time constant(s) of on-chip low-pass filtering and high-pass filtering is (when implemented).

7.5.1.1 Syntax Specification

<AIO pin behavior description> :: = **attribute AIO_Pin_Behavior**
of <component name> **: entity is** <AC pin string> **;**
<AC pin string> ::= **"** <AC pin info list> **"**
<AC pin info list> ::= <AC pin info> { **,** <AC pin info> }
<AC pin info> :: = <AC pin> [**:** <AC/DC select cell>][<time constants>]
<time constants> ::= } [**:** <HP time constant>] [**:** <LP time constant>]{
<AC pin> ::= <port ID>
<AC/DC select cell> ::= <cell number>
<LP time constant> ::= **LP** <time constant>
<HP time constant> ::= **HP** <time constant>
<time constant> ::= <real number>

7.5.1.2 Rules

a) The syntax for the mandatory AIO_ Pin_Behavior attribute shall be that shown above.

b) The value of <port ID> shall contain a <port name> declared in the logical port description for the device.

NOTE – A <port ID> may consist of a <port name> or a <subscripted port name> as described in B.6.3, “Commonly used syntactic elements” in IEEE Std 1149.1-2001. See also B.8.3, “Logical port description statement” in that standard.

c) The value of <port ID> shall refer to a system pin only and not to any pin that is a scan port signal or a compliance port pin; further, the <pin type> of the <port name> shall not be “linkage”.

d) All values of <port ID> elements listed in <AC pin info list> shall be unique.

e) When an <AC pin info> element contains an <AC/DC select cell> element, then the <pin type> of the <port ID> being referenced shall be “out”, “inout” or “buffer” only.

f) The value of <AC/DC select cell> shall be the <cell number> of a Boundary Register cell listed in the <boundary register stmt> with a <function> value of “internal” as recorded in the <cell spec> for that cell.

g) When an <AC pin info> element contains an <AC/DC select cell> element and if the <port ID> identifies a pin that is the <associated port> of a <twin group> in a <grouped port identification>, then the <cell number> value of the <AC/DC select cell> shall be the same <cell number> as that identified in the <AC pin info> element for the <representative port> of the same <twin group> element, and vice versa.

NOTE – This rule cannot be satisfied if one member of a <twin group> has an associated <AC/DC select cell> specified while the other one does not.

h) The value of the <safe bit> element in the <cell spec> for an <AC/DC select cell> shall be “0”.

i) The values of <LP time constant> and <HP time constant> shall be positive real numbers expressing the low-pass and/or high-pass time constants, respectively, of an input pin, in units of seconds.

j) When an <AC pin info> element contains an <HP time constant> and or <LP time constant> element, then the <pin type> of the <port ID> being referenced shall be “in” or “inout” only.

7.5.1.3 Description

The AIO_Pin_Behavior attribute can refer to individual system pins as <subscripted port name> elements or as <port name> elements that refer to individual system pins or collections of system pins. When an <AC/DC select cell> element is associated with a <port ID> element, then any pin(s) so referenced are controlled by that same AC/DC select cell.

Example

```
    attribute AIO_Pin_Behavior of ACDEV : entity is
             "Enable:LP 5.0e-9, Data_bus:9, Cntl(2):32, " &
             "Cntl(1), Addr_bus:HP 1.5e-8:LP 5.0e-9";
```

In this example, port Enable, Data_bus, Cntl(1), Cntl(2) and Addr_bus are all AC pins. Of these, ports Data_bus and Cntl(2) are controlled by internal Boundary Register cells 9 and 32 respectively. The port Enable is an input with a low-pass filter time constant of 5 nanoseconds. The port Addr_bus members each have a low-pass filter time constant of 5 nanoseconds, and each also has an internally implemented AC coupling circuit with a time constant of 15 nanoseconds.

Rule 7.5.1.2g) states that when two AC pins are part of a differential driver pair, then the same AC/DC selection cell (if implemented) must be listed for both of them. This reflects that both pins respond as AC or DC together.

Rule 7.5.1.2h) requires the “safe bit” of an AC/DC selection cell be set to “0”, which becomes a default value for tools that do not compute a value for this cell. This allows tools that are not cognizant of AC testing to assure that AC pin behavior is not selected, even if for some reason they should load either EXTEST_PULSE or EXTEST_TRAIN into a device.

Rule 7.5.1.2i) governs the documentation of the low-pass time constant for a test receiver, if implemented, and documents the high-pass time constant of AC coupling when this coupling is implemented within the device. This allows software to know that a device is AC coupled when the board netlist has no AC coupling devices in a channel, and allows software to compute TCK frequency and/or time spent in the *Run-Test/Idle* TAP controller state. (See section 8.xxx for discussion of T_{Test} times.)

> **Editor’s note:** Need forward reference here to Clause 8 TCK/RTI timing calculations…

7.6 Example BSDL Description

> **Editor’s note:** Need an example IC and BSDL here.

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