P1149.6 Physical and Logical Layers

Discussion fodder: 12/17/01
Overview

• Introduction to structure: “modes” and “layers”
• P1149.6 Physical Layer: Signaling options
  – Differential vs. Dual single-ended
• P1149.6 Logical Layer: Protocol options
  – Timing
  – Frequency
  – Edge
• Comparisons
Vocabulary and Structural Layers

• “Modes”
  – Mission mode (normal operation)
  – Boundary Scan Modes
    • DC Extest mode
    • AC Extest mode

• “Layers” (interface circuits)
  – Mission
  – Physical layer
  – Logical layer (== signaling == protocol)
  – Scan layer
Mission Mode

- Single Tx wire becomes differential data
- AC- or DC-coupled differential interconnect
- Differential receiver produces single Rx wire

**Diagram:**

- **Transmit chip:**
  - Tx_data

- **Receive chip:**
  - Rx_data
Boundary Scan Test Modes

- Data in transmit chip’s Boundary Scan Register(s) must be mapped into (mission) channel data.
- Channel data (mission) must be mapped into receive chip’s Boundary Scan Register(s).

Transmit chip

Receive chip

b-scan

mission

b-scan

CU

CU

CU

CU
Schematic View of Layers (Interfaces)

- **Mission**: functional circuitry
- **Physical**: mission signals ↔ test logic
- **Logical**: (implements protocol) : physical ↔ scan
- **Boundary scan**: (1149.1) : test stim and response

```
transmit chip    receive chip
    b-scan     logical    physical    mission
               CU
               mission    physical    logical
               CU
```
**P1149.6 Physical Layer: Example**

- **Test Driver**
  - Differential drive: use mission driver

- **Test Receiver**
  - Self-referencing hysteretic receiver

*based on IEEE P1149.6:D2.2 p.32, fig 30
P1149.6 Logical Layer: Example*

- **Test Driver**
  - Differential drive: use mission driver
- **Test Receiver**
  - Self-referencing hysteretic receiver

*Throat-clearing driver; Dual-Edge-based receiver
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Physical Signaling Options (6 total)

- Four options for signaling:
  - Differential drive, differential receive
  - Differential drive, dual single-ended receive
  - Dual single-ended drive, differential receive
  - Dual single-ended drive, dual single-ended receive
- Two types of differential receive
  - Mission
  - TestD
1: Diff Dr, Diff Rx (Mission Rx)

+ No driver modification
+ No additional driver noise
- Loss of diagnosability
- 1149.1 compliance issue

+ Leverage mission receiver
- Low diagnosability
- 1149.1 compliance issue
2: Diff Dr, Diff Rx, TestD Rx

+ No driver modification
+ No additional driver noise
- Loss of diagnosability
- 1149.1 compliance issue

- Extra differential receiver
- Low diagnosability
- 1149.1 compliance issue
Diff Dr, Dual SE Rx

+ No driver modification
+ No additional driver noise
- Loss of diagnosability
- 1149.1 compliance issue

- Additional receiver circuits
+ Good diagnosability
+ 1149.1 compliant
4: Dual SE Dr, Diff Rx (Mission Rx)

- Driver modification required
- Driver noise likely
+ Good diagnosability
+ 1149.1 compliant

+ Leverage mission receiver
- Low diagnosability
- 1149.1 compliance issue
5: Dual SE Dr, Diff Rx (TestD Rx)

- Driver modification required
- Driver noise likely
+ Good diagnosability
+ 1149.1 compliant

- Extra differential receiver
- Low diagnosability
- 1149.1 compliance issue
6: Dual SE Dr, Dual SE Rx

- Driver modification required
- Driver noise likely
+ Good diagnosability
+ 1149.1 compliant

- Additional receiver circuits
+ Good diagnosability
+ 1149.1 compliant

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# P1149.6 Physical Layer: Comparison

<table>
<thead>
<tr>
<th>Signaling Technique</th>
<th>+ 1149.1 compliant</th>
<th>- 1149.1 compliance issues</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full differential</td>
<td>+ mitigates ground bounce/noise</td>
<td>+ mitigates ground bounce/noise</td>
</tr>
<tr>
<td></td>
<td>- poor fault coverage and diagnosis</td>
<td>+ good fault coverage and diagnosis</td>
</tr>
<tr>
<td>Diff drive / SE receive</td>
<td>- 1149.1 compliance issues</td>
<td>+ mitigates ground bounce/noise</td>
</tr>
<tr>
<td></td>
<td>+ good fault coverage and diagnosis</td>
<td>+ 1149.1 compliant</td>
</tr>
<tr>
<td>Single-ended / single-ended</td>
<td>+ best fault coverage and diagnosis</td>
<td>- impact on driver design: scalability</td>
</tr>
</tbody>
</table>
Overview

• Introduction to structure: “modes” and “layers”
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• P1149.6 Logical Layer: Protocol options
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• Comparisons
P1149.6 Logical Layer: Purposes

- Connect physical layer to Bscan Register(s)
- Implement circuitry for EXTEST instruction
  - Must be compliant with 1149.1
- Implement circuitry for ACEXTEST instruction
  - Dependent upon protocol chosen (timing, freq, edge)
  - Also dependent upon physical layer (eg. # BSRs)
P1149.6 Logical Layer: Options

- Timing-based (== pattern-based) \{MSA\}
- Frequency-based \{Agilent #1\}
- Edge-based
  - Positive-trigger only \{Philips\}
  - Both edges \{Agilent #2\}
What’s in the green box?

Insert extensive analysis of each proposal here...
# AC EXTEST Technology Comparison*

*tentative

## AC EXTEST Logical Layer

<table>
<thead>
<tr>
<th></th>
<th>Timing-based</th>
<th>Freq-based</th>
<th>Edge-based</th>
</tr>
</thead>
<tbody>
<tr>
<td>New pins?</td>
<td>+ No</td>
<td>- Maybe ?</td>
<td>+ No</td>
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<tr>
<td>Test sig timing</td>
<td>-Skew mgmt</td>
<td>+ Phaseless</td>
<td>+Phaseless</td>
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<tr>
<td>Overhead</td>
<td>+ Medium</td>
<td>- Large</td>
<td>+ Small</td>
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<tr>
<td>Scalability</td>
<td>- At risk</td>
<td>+ Best</td>
<td>+ Good</td>
</tr>
<tr>
<td>Noise</td>
<td>- At risk</td>
<td>+ Immune</td>
<td>- At risk</td>
</tr>
</tbody>
</table>

*December 17, 2001*
## AC EXTEST Technology Comparison*

*tentative

### AC EXTEST Logical Layer

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<tbody>
<tr>
<td>New pins</td>
<td>no</td>
<td>maybe</td>
<td>no</td>
</tr>
<tr>
<td>Si Area</td>
<td>medium</td>
<td>large</td>
<td>small</td>
</tr>
<tr>
<td>Power</td>
<td>?</td>
<td>?</td>
<td>?</td>
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<tr>
<td>Iddq testability</td>
<td>physical</td>
<td>accumulates</td>
<td>physical</td>
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<tr>
<td>Noise immunity</td>
<td>f(skew)</td>
<td>none</td>
<td>none</td>
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<tr>
<td>Max/Min TCK</td>
<td>physical</td>
<td>physical</td>
<td>physical</td>
</tr>
<tr>
<td>Scalability</td>
<td>?</td>
<td>?</td>
<td>?</td>
</tr>
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<td>Tool migration</td>
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<tr>
<td>1149.1 compl.</td>
<td>?</td>
<td></td>
<td>?</td>
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P1149.6 Logical Layer Issues

- Noise Immunity
  - Is any required beyond the Physical Layer?
- Coverage
  - Is there a need for TestD?
- Implementation
  - Scalability to higher frequencies, on-chip Cs
  - Area and extra pins requirements
  - Ease of use via TAP
  - Test time