Title: STIL 1450.3 Internal Review of 1450.3-D04

History:

- 02/01/2002 - issues carried over from D03
- 02/15/2002 - updated from phone meeting
- 04/26/2002 - updated from phone meeting
- 06/21/2002 - updated from phone meeting
- 08/02/2002 - updated from phone meeting

The working document "1450.3-D04) is in the process of being reviewed by the working group. The following individuals have received copies:

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Table 1: Summary of Issues from internal (non-ballot) review of 1450.3

Ident	Issue	Resolution
DF-1 +FM	Request to have suntax defining the status of a tester targeting operation. The idea is to have a new block type called "Violation" that defines any resource problems that occurred when mapping to a given target tester.	2/1/2002: We decided that to add a strict format for error messages would be to go beyond the scope of this project. We cited as precedent that C/C++ language does not specify format of error messages. We also decided that this issue should be listed in the standard as a topic that was considered and purposly omitted. It is so indicated in clause 1, Scope.

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Ident	Issue	Resolution
DF-2	Annex A and B need updating to latest syntax	01/18/2002: Update provided by Dan Fan
DF-3	a) I would like to see we have one more statement to check the "multiple-bit cyclized data" as Section 21.2 of STIL 1450-1999 (page 101) or Section 5.7.2 "Serial Data" (page 39). For clarification, the following are the description in 1450-1999 of "Serial Data": "An alternate representation is also supported in STIL to present serial of stream data. This format is similar to scan data in concept, but is defined as a single vector rather than a sequence of vectors." Our new statement may have syntax such as "MaxData integer_expr". It will allow the ATE vendor to specify how many data bits per vector it can support.	02/01/2002: This issue is covered by the following statements in the WaveformCharacteristics block: MaxData, CompareEvents, DriveEvents.
DF-4	Technical - Need a way of specifying timing resource allocation in a Waveform table. This may be similar in concept to the R/Resource statement as defined for vector-resouce assignment.	*5/16/02 - proposal by Dan being reviewed by wg*
DF-5	Technical - Need a way to specify common tester resources for waveform timing	*6/21/02 - Proposals by DF, JT, TT are being reviewed by wg.*
JD-1	Suggest new clause on Economics.	*Clause 12 has been created as a place holder, awaiting proposal on content from Jason.*
FM-1	Need for an introductory tutorial.	*01/18/2002: Should have several parts to it:* *1. basic STIL file to use as test case (i.e., signals, groups, burst, etc)* *2. set of TRC rules for a (fictional?) ATE system* *3. result of applying the TRC rule (2) to STIL file (1)* *4. resultant STIL file with targeting data included.* *5. simple usage of variables for fluid parameters* *02/15/2002: Identified need for a face-to-face-all-day meeting to work on the tutorial.*

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FM-2	Suggestion to move Site and Port out of the Pattern block.	01/18/2002: This led to a big discussion with regard to the purpose and scope of 1450.3 and in particular all the ways that TRC fits in to the usage model in figure 1. There was not clarity on how all these application fit together and whether the syntax can be clear for each usage. For example: Site and Port may make sense when defining the resources of an ATE system, but not when reporting the statistics of a pattern. 02/01/2002: Figure 1 was updated for clarity. *02/15/2002: There is still debate as to whether the Port and Site commands should be in Economics block or a System block. Needs wg decision.In either case wg does NOT like it in the Pattern block.* *4/26: Get input from the 1450.4 effort on multi-site before deciding. (see also TT-1)*

JT-1	I noticed that you added an example for multisite in clause 11. I brought up a comment about ping-pong and agreed to do an example:
	
	 NameMaps MultiSite_pingpong {
	   SIG1 "INPUT (13 48) (96 106)";
	   SIG2 "BIDI (45 83) (99 107)";
	   SIG3 "OUT (46 85) (128 126)";
	 } // end NameMaps MultiSite_pingpong
		02/01/2002: This code is added to the example.

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Ident	Issue	Resolution
JT-2	a) 14.1 para (5) What is the reason for this value? It seems like this is specified in a tester implementation specific manner. The Credence DUO/Quartet series testers don't have a capture memory, or you could might say that the capture memory depth is 1. But, would stating that the capture memory is 1 cause some tool to believe that a part couldn't be tested on this tester? There is no limit to the number of errors that can be logged on this tester. The error detection mechanism is neither FailOnly nor Result, but something called error history which is a 48 bit ring buffer that captures pass and fail on each cycle. I do think that we need to have a parameter that specifies the maximum number of errors that can be captured on a burst. The way the Credence system captures errors there is a performance hit because the burst has to be re-run. This could be included in the economics section when we figured out what that is. b) This also bring to mind that there are some bursts that can't be re-run without first doing some pre-conditioning of the part, such as cycling the power. Do we have a way to capture this?	a) 02/01/2002: Syntax was discussed at working group meeting and decided to leave as is. If there is no limit to capture memory, this can be specified by integer=-1. b) 02/01/2002: This issues can be addressed in several ways - The pattern itself can contain the preconditioning sequence. A PatList can contain the pre-conditioning pattern. The flow (p1450.4) can define the sequence requirement.
JT-3	clause 16.1 Is there away to specify a maximum frequency for scan vectors?	02/01/2002: This is done by placing scan signals and data signals in separate Signals blocks and thereby defining unique characteristics of each, including the PeriodCharacteristics block that is referenced.
JT-4	a) clause 17.1 para 2 & 20 This is just a request. Could we put accuracy and resolution next to each other in the spec? b) clause 17.1 para 18 - MinStrobeWindow I think there two types of compares, window compare and strobe compare. Window compares start with an edge and end with an edge. If at any time during the window the voltage drops below the compare level it fails. A compare strobe is a single edge which does a point compare. If the voltage is below the compare level at that point it fails. For window compares there are minimum times for windows and minimum times between windows. For strobe compares there are minimum times between strobes.	a) The statements are all alphabetical. b) 02/01/2002: Changed MinStrobeWindow to MinCompareWindow. The minimum time between edge strobes is specified with the MinEdgeRetrigger statement.

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JT-5	a) Clause 19 sections to be added. Add a MaxLoopIteration. This is the maximum number of iteration that a loop can have. Add a MinLoop-Length and MaxLoopLength. Add a MaxNumberCycles. This is the number of cycles a tester can execute on a single burst. This is usually much larger than the maxVectors. Can repeats occur within loops? What is the minimum separation between loops? What is the minimum separation between repeats? Is there an interaction between the min separation of loops and the min separation of repeats? Does the min separation of repeat apply, if the repeat count is the same? What is the min separation of scan? Is the min separation of scan affected by loop and repeat? Are there boundary start and stop conditions for loops, such as loops can only start and stop on 8 vector boundaries? Is there a loop-until-advance? This is an infinite loop that is broken out of when a register is written to. Match loops can have some additional restrictions such as, the number of vectors before of after the loop where failures must be masked, and areas at the beginning and ending of the loop where failures must be masked. b) Multi-time domain - Are there constraints on how often multi-time domain signals must sync up. For example, can the tester handle 4 time domains where the frequencies are 51,52,53, & 99 MHz?	a) 02/01/2002: The syntax for MaxLoop and MaxLoopNest is to be revised to see how many of these additional constraints can be covered. Proposed syntax added to the doc. 8/2/2002: tt - clause 18 has been updated with enhanced syntax for InstructionCharacteristics and LoopCharacteristics. b) 02/01/2002: Re-synchronization is a function of the way the separate patterns are constructed. If explicit waiting is to be done between patterns, then this should be addressed by a UserFunction within the patterns.
JT-6	clause 19.1 para 17 - "i.e., the number of different devices that can be tested in parallel." Is this correct, or is this really for multi-time domain testing on a single part.	02/01/2002: This issue is addressed by improved wording in the Multi-Port statement.

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TT-1	If multiple rules are defined in a STIL file, should they be contained in separate Environment blocks or separate TRC blocks within one environment.	4/26: wg decision that only one set of rules should be within an Environment block. Wg recognized that it is possible to use variables to create one set of rules that supports a family of testers. See also FM-2 about having a System block. 7/16: Added a new clause 7 defining the structure of various applications of TRC. *needs wg review*
TT-2	Technical - Need a mechanism for encrypting a rules file.	4/26: wg decided that a new section (perhaps an annex) should be added to say that this is outside of the scope of the standard, but should be done using standard encrypting tools on a per file basis. *tt - update the doc*
TT-3	Editorial - Need to identify potential TRC errors that can occur when a pattern file is compared to a set of TRC rules.	*5/19/02: See examples that have been added to the document. Additions have been made in the syntax definition clauses with the identifier "TRC-ERR" on each line.*
TT-4	Editorial - Need to enhance the examples in each syntax section to contain an example of each statement and make them complete/compilable.	
TT-5	Technical - Need a statement to specify the maximum length of a scan chain. This is most important in: a) specifying a resource constraint on a design/too, or b) specifying in a pattern report.	*6/14/02: Added Signals -> MaxScanChainLength.* *- need wg approval*
TT-6	Annex E needs updating.	*AI: Tony*
TT-7	Need a way to encrypt a TRC file. ATE vendor may want to control the availability of the data.	*4/26/02 - Decided to add writeup to the doc to say that it should be done using standard industry available encrypting tools on a per file basis.* *tt - update the document*
WG-1	What are the requirements for ordering of blocks in a TRC file.	*02/01/2002: This specification is to be added. It is recognized that many parsers now create all blocks (with exception of pattern blocks) into memory and can inherently handle forward references. AI-tony.*