STIL .4 Doc Restructuring Proposal

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Effort Motivations:

1. Establish top-level chapters using syntax block names for easy user navigation
2. Ensure that each syntax block has syntax and example sub-chapters
3. Identify changes to previous extensions referencing clause with proposed modifications
4. Remove chapters that are out of scope
5. Fulfill action item from 10/7/2014 committee meeting

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Annex A..?

**Proposed Chapters for Removal:**

**Chapter Reason**

6.2 Comments *Addressed in .0*

6.3 Token Length *Addressed in .0*

6.5.3 DCSequence *Addressed in .0*

6.5.4 Wafer Map *Not in Scope*

6.5.5 Prober/Handler Interface *Not in Scope*

6.5.6 Multi-site/MPW Testing *Managed by ATE O/S, not language*

6.6.4 Capture Memory and Analysis *Not in Scope*

6.9.5 Bin Axes *Not practical for SPC or Yield systems*

6.9.7 Bin None *Managed by ATE O/S, not language*

6.9.9 Counters *Defined by Production, Not Test Pgm*

6.9.10 Retest *Defined by Production, Not Test Pgm*

6.11 Interaction with Other IEEE 1450 Extensions *Addressed in .0*

6.12 Input File Organization *Addressed in .0*

# Overview

## Scope

## Purpose

# References

# Definitions

# Preface

# Tutorial

# Extensions to Clause 6.3 "Reserved words"

# Extensions to Clause 8 "STIL statement"

## STIL syntax

## STIL example

# SignalMap

## SignalMap syntax

## SignalMap example

# FlowVariables

## FlowVariables syntax

## FlowVariables example

# Bin

## Bin syntax

## Bin example

# SoftBinDefs

## SoftBinDefs syntax

## SoftBinDefs example

# HardBinDefs

## HardBinDefs syntax

## HardBinDefs example

# BinMap

## BinMap syntax

## BinMap example

# Flow Conceptual Model

# Test

## Test syntax

## Test example

# FlowNode

## FlowNode syntax

## FlowNode example

# Flow

## Flow syntax

## Flow example

# TestProgram

## TestProgram syntax

## TestProgram example

# Device

# Global Functions

# Standard Definitions