

STIL .4 Doc Restructuring Proposal
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Effort Motivations:

1. Establish top-level chapters using syntax block names for easy user navigation
2. Ensure that each syntax block has syntax and example sub-chapters
3. Identify changes to previous extensions referencing clause with proposed modifications
4. Remove chapters that are out of scope
5. Fulfill action item from 10/7/2014 committee meeting

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Proposed Chapters for Removal:

Chapter	Reason
6.2 Comments	<i>Addressed in .0</i>
6.3 Token Length	<i>Addressed in .0</i>
6.5.3 DCSequence	<i>Addressed in .0</i>
6.5.4 Wafer Map	<i>Not in Scope</i>
6.5.5 Prober/Handler Interface	<i>Not in Scope</i>
6.5.6 Multi-site/MPW Testing	<i>Managed by ATE O/S, not language</i>
6.6.4 Capture Memory and Analysis	<i>Not in Scope</i>
6.9.5 Bin Axes	<i>Not practical for SPC or Yield systems</i>
6.9.7 Bin None	<i>Managed by ATE O/S, not language</i>
6.9.9 Counters	<i>Defined by Production, Not Test Pgm</i>
6.9.10 Retest	<i>Defined by Production, Not Test Pgm</i>
6.11 Interaction with Other IEEE 1450 Extensions	<i>Addressed in .0</i>
6.12 Input File Organization	<i>Addressed in .0</i>