1450.4 meeting minutes – 02/27/13

Attendees: Ernie Wahl, Jim O'Reilly, Mitsuo Fujii
Not present: Julia DiChiaro, Oleg Erlich, Markus Seuring, Ajay Khoche, Paul Reuter

Summary:

Line numbers are from syntax document dated February 26, 2013

- Line 763: Added Signals and SignalGroups reference statements to Chip block to allow per-chip definitions
- Line 776: Changed SignalMap to ChannelMap (maps named for mapping-to to distinguish ChannelMap from PinMap)
- Line 790: Added PinMap to pkg_attribute and move Pin statement from Signal to here
- Line 3826: Changed sig_type to sig_type_stmt, defined sig_type_stmt below and explained sig_type combination
  - Syntax had not fallen in line with stated intent, i.e., use sig_type in combination
- Line 3848: Added sig_type FreeClock, need to settle on clock speed specification syntax
- Line 3908: Added IDD ACCURACY parameters to Power keyword to help ATPRG
  - determine power channel configuration. Optional IDD and ACCURACY represent the nominal current draw and the most lenient accuracy to which it may be measured. These parameters enable an ATPRG to configure target tester power channels.
- Line 3934: Added "(Specs VARIABLES_BLOCK_NAME;)"
  - Augments, e.g., "(Power PWR_SIG_NAME (,PWR_SIG_NAME)*;)", IIL, IIH, etc. which require literal values Variable block provides tracking statements and reuse, e.g., variable block named TTL may be applied all TTL signals

Reference documents (If logged into your google account, can edit. If not, can only view.)

- Current Draft Syntax Document
- Issues List
- Namespace resolution examples document
- Communications spread sheet (scratchpad spreadsheet)
- Communications word doc (scratchpad word document)

Next meeting: 03/05/13

For reference STIL .4 information can be found at the IEEE STIL website: http://grouper.ieee.org/groups/1450/
(select the P1450.4 link from the table) or use the direct link http://grouper.ieee.org/groups/1450/dot4/index.html