1450.4 meeting minutes – 03/06/13

Attendees: Ernie Wahl, Jim O'Reilly, Mitsuo Fujii, Markus Seuring
Not present: Julia DiChiaro, Oleg Erlich, Ajay Khoche, Paul Reuter

Summary:

Line numbers are from syntax document dated March 5, 2013

- Line 772: discussed per-chip Signals/SignalGroups block definitions (as opposed to per-chip references to external/global defined Signals/SignalGroups blocks). No conclusion. Define-before-use remains intact in either case.
- Discussed Fujji-san email dated Mon 3/4/2013 5:15 AM:
  - Item 4: concluded that ForceMode (VSIM | ISVM(and MeasMode (Serial | Multi) are best served via STIL.5 TestType definitions and temporarily via non-standard TestType definitions. Awaiting feedback. STIL.4 has no target tester channel configuration syntax. STIL.2 does but appears insufficient for this purpose.
  - Item 5: current syntax is define before use.
  - Item 6: closed.
    - "... meaning among describing orders of Power rails and IOH levels etc. in stil4_attribute". How do we describe such correspondence between Power and buffer capabilities in STIL.4?
    - From Syntax document dated March 5, 2013, section 6.10.1.3 "Signals and SignalGroups", p108, paragraph on *buf_attributes*: The number of values associated with these keywords shall match the number of Power signals. The number of values associated with these keywords shall match the number of Power signals. There is positional correspondence so for the following statements:
  - Item 7: FreeClock:
    - agree that FreeClock needs a place in the syntax (there are other circuit requirements of similar nature, e.g., pullup(50R), CTap(10uF), etc.). Signal associated circuit requirements ought to translate into applied tester resources or loadboard components. STIL.0 lacks WaveformTable syntax for FreeClock (can't specify asynchronicity).
    - agree specifying period or frequency.
    - agree specifying timing domain via arbitrary tag.
    - start/stop is unresolved:
      - we have capability via data-type VecLocation but aren't sure that this is appropriate.
      - start/stop is usually specified in the pattern (via in-pattern syntax currently lacking in STIL.0).
      - this looks like mixed-signal testing which was not part of STIL.4 PAR,certainly not phase I (phase II is a possibility). STIL.4 identifies analog signals well enough to determine whether they can be tested in any way on a digital tester but goes no further. STIL.7, now dormant, also seems like an appropriate forum.

Reference documents (If logged into your google account, can edit. If not, can only view.)

- Current Draft Syntax Document
- Issues List
- Namespace resolution examples document
- Communications spread sheet (scratchpad spreadsheet)
- Communications word doc (scratchpad word document)

Next meeting: 03/12/13

For reference STIL .4 information can be found at the IEEE STIL website: http://grouper.ieee.org/groups/1450/ (select the P1450.4 link from the table) or use the direct link http://grouper.ieee.org/groups/1450/dot4/index.html