

1450.4 meeting minutes – 06/27/12

Attendees: Ernie Wahl, Jim O'Reilly

Not present: Julia DiChiaro, Oleg Erlich, Markus Seuring, Ajay Khoche, Paul Reuter

No teleconferences were held on Jun 13, June 20.

Administrative Summary:

New PAR for P1450.4 was approved at the IEEE-SA NESCOM meeting on June 7. This new PAR is now posted on our P1450.4 website..

Summary:

Line numbers are with regard to syntax document dated June 5, 2012.

- ACCEPT: Update section "1.1 Scope" text (Lines 363 - 372) with text from PAR.
- ACCEPT: Update section "1.2 Purpose" text (Lines 375 – 382) with text from PAR.
- ACCEPT: (ref Fujii-san email dated June 21, 2012)
 - Item 1: substitute acronym ATPRG (Automatic Test PRogram Generator) for acronym ATPG throughout document. Established usage of ATPG represents Automatic Test Pattern Generator.
- ACCEPT: ref Fujii-san email item 2, email lines 738-740

```
738      (Sites SITE_COUNT (SITE_LAYOUT_NAME) (: site_layout) {
739          (SIG_NAME (CHAN_ID (,CHAN_ID)); | SIG_NAME (CHAN_ID (,CHAN_ID)) { (sig_attribute)* })*
740      })+ // Multi-site testing shall requires multiple Sites blocks under our Site definition in next item 3.
```

COMMENT:

Allow multiple **Sites** blocks, but within each **Sites** block, only one optional SITE_LAYOUT_NAME is allowed (SITE_LAYOUT_NAME can appear 0 or 1 time only. Fujii-san's syntax showed the following for line 738:

```
738      (Sites SITE_COUNT (SITE_LAYOUT_NAME)* (: site_layout) {
```

which would allow SITE_LAYOUT_NAME to appear any number of times (or not at all) – and we believe the intent is to allow SITE_LAYOUT_NAME to appear 0 or 1 time only within a **Sites** block

QUESTION for SCSWG: What purpose is served by allowing more than one SITE_LAYOUT_NAME per site_layout ? Ref email line 738 above

- ACCEPT: ref Fujii-san email item 2, email line 743:

```
743 })+ // Added right brace and bracket
```

COMMENT: accentuates divergence between Design and Tester blocks, i.e., zero or one Design block but one or more Tester blocks are acceptable. **Conclusion: separate syntax descriptions required for Design and Tester blocks.** ATPRG may use Design block plus additional information to generate Tester blocks. Proposed syntax for Design and Tester blocks is as follows:

PROPOSED:

```
(SignalMap MAP_NAME {
    (Components { (element_statement)* })
    (Device DEVICE_NAME {
        (Chip CHIP_NAME; | Chip CHIP_NAME { ( Site SITE_NR (, SITE_NR)*;) } )+
        (Package PACKAGE_NAME; | Package PACKAGE_NAME { (pkg_attribute) })
        (Design {
            (SIG_NAME { (sig_attribute)* })*
        })
        (Tester TESTER_NAME {
            (Components { (element_statement)* })
            (Sites SITE_COUNT (SITE_LAYOUT_NAME) (: site_layout) {
                (SIG_NAME CHAN_ID (,CHAN_ID)*; |
                SIG_NAME CHAN_ID (,CHAN_ID)* { (sig_attribute)* })*
            })+
        })+
    })+
})+
```

- Ref Fujii-san email item 2, email line 748:

```

748 buf_attribute = Type TYPE_NAME; |
                    (Power PWR_RAIL_NAME (, PWR_RAIL_NAME)*;) |
                    (Ground GND_RAIL_NAME (, GND_RAIL_NAME)*;) |
                    (Direction < In | Out | InOut | Power | Ground >;) |
                    (Drive DRIVE_TYPE_NAME (, DRIVE_TYPE_NAME)*;) |
                    (Structure STUCTURE_TYPE_NAME (, STUCTURE_TYPE_NAME)*;) |
                    (IsConnected INTENAL_CORE_PIN_NAME INTENAL_CORE_NAME
                     INTENAL_CORE_INSTANCE_NAME
                     (, INTENAL_CORE_PIN_NAME INTENAL_CORE_NAME
                     INTENAL_CORE_INSTANCE_NAME)*; |
                     (User USER_DEFINED (, USER_DEFINED)*; )

```

ACCEPT additions (, PWR_RAIL_NAME)* and (, GND_RAIL_NAME)*

COMMENT (EJW): Regarding keyword "IsConnected": we appreciate the utility of mapping an external signal to one of a number of core signals. For this to be useful, we need to know which pattern (or vector location) puts a particular mapping into effect.

COMMENT (EJW): We've had minimal discussion regarding keyword "User". Con: STIL.0 already provides "UserKeywords". Pro: context dependent keyword "User" is more efficient than "UserKeywords" which once defined, requires that each user-keyword be recognized in every context where a STIL statement may occur.

NOTE (EJW): STIL.4 may adopt STIL.1 context dependent "UserKeywords" specification since it is unadvisable to mix STIL.4 and STIL.1 code.

- Questions with regard to Fujii-san email:
 - Ref Fujii-san email item 2, email line (Q2-4):

```

748 buf_attribute =
    Type TYPE_NAME; |
    (Power PWR_RAIL_NAME (, PWR_RAIL_NAME)*;) |
    (Ground GND_RAIL_NAME (, GND_RAIL_NAME)*;) |
    (Direction < In | Out | InOut | Power | Ground >;) |
    (Drive DRIVE_TYPE_NAME (, DRIVE_TYPE_NAME)*;) |
    (Structure STUCTURE_TYPE_NAME (, STUCTURE_TYPE_NAME)*;) |
    (IsConnected INTENAL_CORE_PIN_NAME INTENAL_CORE_NAME
     INTENAL_CORE_INSTANCE_NAME
     (, INTENAL_CORE_PIN_NAME INTENAL_CORE_NAME
     INTENAL_CORE_INSTANCE_NAME)*; |
     (User USER_DEFINED (, USER_DEFINED)*;)

```

COMMENT (EJW): The proposed attributes appear to be a mixture of buffer-type and buffer-instance attributes. To date, the STIL.4 committee has determined that buffer-type attribute definitions are outside the scope of STIL.4. We expect buffer-type attributes to be stored in a buffer-type library format of the vendor's choosing. Particular buffer-type attribute may be found in that library via the buffer TYPE_NAME. Buffer-instance attributes described in STIL.4 are designed to override buffer-type information, e.g., when a buffer's full capabilities need not be tested. Buffer-instance attributes may also be used to supply minimal information when an ATPRG has no access to a buffer-type library.

Q2: Does "(Direction < In | Out | InOut | Power | Ground >;)" serve a purpose for buffer-instance considering that the STIL.0 Signals block already describes these and other attributes ? See STIL.4 section "7.9.1.3 Signals and Signal Groups" for additions to STIL.0 syntax.

NOTE (EJW): I expect that the buffer-type library would associate this attribute with a particular buffer-type pad. An ATPRG can use the library to generate a default Signals block which the user may alter before a target test program is generated.

Q3: Regarding keyword "Drive" followed by ad-hoc strings: would you be open to instead specifying IIH, IIL, IOH, IOL, IOZH, IOZL, VIH, VIL, VOH, VOL with standard format parameters ?

Examples of such a specification:

```
IOH 8mA, 16mA, 24mA, 32mA; // For 4-state programmable buffer
VIH 2.0V;                  // TTL specified as a literal
VIH VIH_TTL;               // TTL specified as a variable
```

COMMENT (EJW): N-state programmable buffer requires additional state information: signal-state to current-capability mapping. If static (hardwired), need current-capability selection. If dynamic (runtime programmable), require vector location for each current-capability specification.

Q4: Regarding keyword "Structure": this appears to be an unalterable property of a buffer-type pad, i.e., belongs in the buffer-type library. If you are comfortable with the decision that buffer-type libraries are outside the scope of STIL.4, there is no need for further discussion (you control your own library format). If you are not, we need to fit this into our time-table (we are hoping to go to ballot near year end and this may be a major undertaking depending on how comprehensive we'd intend to be). What is your position ?

Q5: Regarding the use of the word "Site": would you be open to using the word "Partition" instead ? The word "Site" has the long established meaning of referring to a piece of real estate on a wafer occupied by a device so using it for other purposes will likely cause confusion. We're toying with the idea of adding keyword "Partition" before keyword "Sites" in the "Tester" block:

```
(Partition PARTITION_NAME {
  (CHAN_ID;)+
}) *
Example for a one signal (SIG_A) device:
SignalMap sigmap {
  Device simple {
    Chip simple;
    Tester T2000 {
      Partition SiteController1 {
        1.1; // Channel 1.1 is controlled by SiteController1
      }
      Partition SiteController2 {
        40.1; // Channel 40.1 is controlled by SiteController2
      }
      Sites 2 {
        // Site 1 controlled by SiteController1
        // Site 2 controlled by SiteController2
        SIG_A 1.1, 40.1;
      }
    }
  }
}
```

If this works for Advantest, we'll have to check if this is a reasonable representation for other ATE manufacturers as well.

NOTE: Discussions about multi-site issues are ongoing with SCSWG

Actions:

- Jim to rework Verigy example from STIL paper so that the STIL translation is consistent with its original Verigy code.

Reference documents (If logged into your google account, can edit. If not, can only view.)

- [Current Draft Syntax Document](#)
- [Issues List](#)
- [Namespace resolution examples document](#)
- [Communications spread sheet](#) (scratchpad spreadsheet)

- [Communications word doc](#) (scratchpad word document)

Next meeting: 07/10/12 (Teleconferences cancelled Jul 4, 2012, due to US holiday)

For reference STIL .4 information can be found at the IEEE STIL website: <http://grouper.ieee.org/groups/1450/>
(select the [P1450.4](#) link from the table) or use the direct link <http://grouper.ieee.org/groups/1450/dot4/index.html>