

1450.4 meeting minutes – 09/05/12

Attendees: Ernie Wahl, Jim O'Reilly

Not present: Julia DiChiaro, Oleg Erlich, Markus Seuring, Ajay Khoche, Paul Reuter

Summary:

Line numbers are with regard to syntax document dated September 04, 2012

- Line 731: tentatively ACCEPT Wafer block with the following elements which need to be vetted:
 - Wafer Size: e.g., 8" 12"
 - Minimum Pad Pitch: e.g., 400um, distance between centers
 - Minimum Pad Size: e.g., 90um, smallest distance across pad
 - Pad shape: e.g., bump, square, etc.
 - Number of Rows: e.g., 6
 - Number of Columns: e.g., 10
 - X Size: e.g., 20780um, stepping distance (die size + street width) ?
 - Y Size: e.g., 30960um, stepping distance (die size + street width) ?
 - First Row: e.g., 1
 - First Column: e.g., 1
 - X Origin: e.g., -390um, with respect to upper left 6x10 rectangle ?
 - Y Origin: e.g., 3480um, with respect to upper left 6x10 rectangle ?
 - Legend: e.g., A = device_name_a, B = device_name_b, (space is vacant site)
 - Map:

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- Line 788: VERIFIED pkg_attribute syntax

NOTE: Discussions about multi-site issues are ongoing with SCSWG

Actions:

- Jim to rework Verigy example from STIL paper so that the STIL translation is consistent with its original Verigy code.

Reference documents (If logged into your google account, can edit. If not, can only view.)

- [Current Draft Syntax Document](#)
- [Issues List](#)
- [Namespace resolution examples document](#)
- [Communications spread sheet](#) (scratchpad spreadsheet)
- [Communications word doc](#) (scratchpad word document)

Next meeting: 09/12/12

For reference STIL .4 information can be found at the IEEE STIL website: <http://grouper.ieee.org/groups/1450/> (select the [P1450.4](#) link from the table) or use the direct link <http://grouper.ieee.org/groups/1450/dot4/index.html>