The Intelligent Approach to Intellectual Property

An IP Providers Perspective
- IEEE P1500 Meeting-

Mark Payer
Technical Marketing Manager
IP Division
Agenda

- DFT for Soft Cores
- DFT for Hard Cores
- DFT for Firm Cores
- SOC DFT Solutions
- What we need from P1500
- Our commitment
We know what we provide

- Around 100 soft cores
  - Microcontrollers, Peripherals etc
  - DSP functions
  - Communication functions
  - etc etc
- Memories
- Physical libraries
- Datapath libraries

But we can’t predict how they will be used ….
The SOC design process

- **Architecture**
  - Selecting cores
  - Partitioning between hardware and software

- **Integration**
  - Putting IP and other blocks together

- **Implementation**
  - Turning the design into production silicon

DFT affects integration and implementation
What is our soft core DFT strategy?

iscard

- We supply RTL
  - Synthesised to any technology
  - Used as a functional black box
- We ensure that the cores are straightforward to scan test
  - User can then test without knowledge of function
  - We provide information key to DFT tools
  - Core will work with other tools - e.g. Logic BIST
- User synthesises into target technology and inserts scan
Is this always good enough?

- **Aim of using IP is to speed time to market**
  - Soft cores need to be implemented
  - Soft cores are not characterised

- **One solution to offer Firm Cores**
  - Implementation is more deterministic

- **Another solution is to offer Hard Cores**

- **Our solution is a ‘hardening service’ for soft cores**
  - Solves the implementation problem
    - The integration problem remains
What is our hard core DFT strategy?

- We supply hard cores with appropriate DFT solution implemented (Structures + vectors)
  - Legacy (non-scan), Scan Test, Logic BIST

- Advantage:
  - User has a ready-made solution which is characterised for timing area

- Disadvantage:
  - User still has to merge it with the DFT structure of the rest of his chip
    - Hence the need for DFT standards!
Hard Core Reality

- Hard cores are not portable
  - Limited application space
- Hard cores have limited life
  - Silicon Technology moves on
- We need to offer a cost effective ‘hardening’ service
  - Requires a standard flow
Firm Core DFT strategy

- **A Firm Core is:**
  - Netlist in a target technology
  - Block or detailed placement (.def, .pdef)
  - Scan-chain inserted
  - Timing back-annotated

- **Main advantage is increased predictability**

- **DFT solution more or less implemented**
  - But may need to fit in with DFT approach for rest of design
Delivering a solution

- There is no point in delivering IP unless there is a reasonable production test solution.
- We have partnered with the Mentor DFT tools group to develop a SOC test solution.
- Mentor DFT tools group active in P1500.
- Commercial DFT products will result:
  - Core BIST
  - CTI
Core Test Integrator Flow

Core Provider

Core Test Description

RTL Synthesis (Access & Isolation)

Logic Synthesis

Design Rule Checking

Test Vector Translation

SOC Test Vector Set

Test Coverage Report

SOC RTL Netlist

Core Integrator

Mentor Graphics

The Power to Create
SOC Snags

- Scan volume becomes too great
- BIST Structures
  - Cut down vectors
  - Add area overhead
- Solution is:
  - One controller for all logic cores
  - One controller for all memories
  - Use test buses
Core BIST Structure
Non-Scan Core Test Structure
MBIST Test Bus Structure
System ASIC DFT Architecture

- Boundary Scan
- Test Access and Support
- Memory BIST
- Logic BIST
Too many buses

- Too many buses
  - Logic Test, Memory Test, System, Emulation ....
- Leads to routing congestion and over-complication
- Why not combine test and on-chip interconnect buses?
DFT Support for hierarchical cores

- Today’s chip is tomorrow’s core
- If a soft core - can treat as one block from the functional RTL point
  - i.e. Re-Scan or Re-BIST
- If a firm or hard core - will have to use the original chip test solution
- Points to a need to have a hierarchical test architecture
Hierarchical Core Test

2nd Generation Core

1st Generation Core

Test Control I/F

Test Control I/F

3rd Generation Core

Test Control Interface

Test Access
What we need from the P1500 standard

- A test bus that can map onto an on-chip bus structure
- Hierarchically expandable test control
- Standard approaches for:
  - Supporting test structures
  - Defining how to isolate cores, or control TRI-States
  - Defining how to initialise cores
- We need this to build standard interfaces and support for the standard test language into our product database
Our commitment

To_serve_our_customers: PROCESS( )
BEGIN
  IF (P1500 = STANDARD) THEN
    We_adopt_P1500;
  ELSE
    We_adopt_the_established_standard;
  END IF;
END PROCESS;