IEEE P1500 Scaleable Architecture Task Force Status Update

January 28, 1998
Task Force Status Topics

- General Task Force Update since ITC98
  - Active Task Force Members
  - Updated Task Force Operating Model
  - Preview of Overall Architecture
  - Review of Task Force Basic Principles
  - Core Test Requirements
  - Presentations & Discussion Topics Since ITC98
Active Task Force Members

Lee Whetsel (Task Force Chair) - Texas Instruments

Saman Adham - Nortel
Sandeep Bhatia - AMBIT
Debashis Bhattacharya - TI
Dwayne Burek - LogicVision
C.J. Clark - Intellitech
Mike Collins - Cisco Systems
* Grady Giles - “Home Alone Inc.”
Alan Hales - Texas Instruments
Erik Jan Marinissen - Philips
Teresa McLaurin - Motorola
Jim Monzel - IBM

Fidel Muradali - Hewlett-Packard
Janusz Rajski - Mentor Graphics
Rochit Rajsuman - Advantest
Mike Ricchetti - Synopsys
David Stannard - Mentor
Jon Udell - Palmchip
Norbert Valverde - Intellitech
Prab Varma - Veritable
Sitaram Yadavalli - Intel
Alex Zamfirescu - ASC
Yervant Zorian - LogicVision
Updated Task Force Operating Model
Phase 1 - Digital Core Test Development

Start Digital Phase

Development of Scalable P1500 Architecture for Cores without 1149.1

Proposals & Ideas

Development of Scalable P1500 Architecture for Cores with 1149.1

End Digital Phase

Wrapper Cells
- Shared
- Non-Shared
- Rippling
- Non-Rippling
- With PI
- With PO
- With PI&PO

Compatibility Checker

Features
- Core Test Access
- Core Interconnect
- Core Isolation
- Hierarchical Reuse

Protocols
- Capture/Shift
- Capture/Shift/Update
- Delay Test
- Runbist

Instructions
- CSP Based
- TAP DR Based
- TAP IR Based

Controllers
- TAP
- Non-TAP
- Extest
- Runbist
- Sample
- Preload
- Enable PIO
- Scan

January 28, 1999
Development of Scalable P1500 Architecture for Cores without P1149.4

Development of Scalable P1500 Architecture for Cores with P1149.4

Compatibility Checker

Wrapper Cells
- TBD

Features
- TBD

Protocols
- TBD

Instructions
- TBD

Controllers
- TBD

Proposals & Ideas

Updated Task Force Operating Model
Phase 2 - Mixed Signal Core Test Development
Preview of Overall Architecture

User Defined Test Access Mechanism

Standardized Core 1
P1500 Wrapper

Standardized Core N
P1500 Wrapper

IN
FI
PI
PO
Enable
PI
PO

FO
FI

SI
Control
SO

OUT

System Chip

IEEE Embedded Core Test
Review of Task Force Basic Principles

1. Embedded core test requires the following hardware components:

   (1) A Wrapper (around the core)
   (2) A Source/Sink for test patterns (on or off-chip)
   (3) An on-chip Test Access Mechanism (TAM) to connect the Wrapper
to the Source/Sink.

2. P1500 is meant to facilitate test reuse for "non-merged" cores.

3. The P1500 Scalable Architecture should define the behavior of a
   standard Wrapper per core and its interface with the Test Access
   Mechanism (TAM).
4. The standard Wrapper behavior will facilitate:
   (1) Core Functional Mode - (core is functional)
   (2) Core Test Mode - (core is tested)
   (3) Core Interconnect Test Mode - (I/O’s between cores are tested)
   (4) Core Isolation Mode - (core I/O’s isolated)
   (5) Control for switching between the modes - (via a Control Scan Path (CSP))

5. The standard Wrapper of a core may interface with 4 types of Input/Output signals:
   (1) Static control signals for Wrapper modes - (instruction loaded into CSP)
   (2) Digital data and dynamic control signals (to be routed through Wrapper cells)
   (3) Exceptional signals (such as analog and "special-care” signals) may bypass the wrapper.
   (4) Dynamic Control signals to operate the CSP and Wrapper Cells
Review of Task Force Basic Principles

6. The standard Wrapper behavior may be: (1) Implemented and provided by core vendors, or (2) added to the core during a subsequent design stage. It is assumed that EDA vendors will: (1) offer tools to implement the standard Wrappers, (2) check for compliance, and (3) provide system-chip level optimization.

7. The interface between the Wrapper and Test Access Mechanism will be standardized, but not the specific Test Access Mechanism of the system-chip. The Test Access Mechanism used will depend on the system-chip test requirements.

8. The P1500 standard will define how both 1149.1 & non-1149.1 cores can co-operate during test.
9. The P1500 Scalable Architecture will specify the standard Wrapper and the interface to the Test Access Mechanism, the description of which will be specified by the P1500 Core Test Language (CTL) and be included in the core test standard information model (along with test patterns, internal DFT, etc).

10. The P1500 standard should be applicable to hierarchical cores.
Core Test Requirements
Required Modes for Embedded Core Test

Core Normal Mode
- Allows core to function normally

Core Test Access Mode
- Allows pre-computed test patterns to be applied to core

Interconnect & User Defined Logic (UDL) Test Access Mode
- Allows testing of interconnect and UDL between cores

Test Isolation Mode
- Allows core to be isolated when it or a neighboring core/UDL is tested.
Core Test Requirements
Basic Wrapper Test Input Functions

- Basic Wrapper Test Input Functions:
  - **Input Observation**: Observation of values which are applied to core inputs from outside of the core.
  - **Input Control**: Applying test data to core inputs so that it can be propagated into the core.
  - **Input Constraint**: Forcing core inputs to fixed values to prevent damage to the core, reduce its power consumption, etc...
Core Test Requirements

Basic Wrapper Test Output Functions

- **Output Observation**: Observation of values which are propagated to core outputs from inside the core.

- **Output Control**: Applying test data to core outputs so that it can be propagated to the logic outside the core.

- **Output Disable**: Forcing 3-State core outputs to their inactive state to prevent damage to other three-state drivers on the same bus.

- **Output Constraint**: Forcing Non-3-State core outputs to fixed values to prevent damage to the logic outside of the core, reduce its power consumption, etc.
Core Test Requirements

Summary of Core Test Capabilities

- **Core Normal Mode**
  - Wrapper is transparent, core functions normally

- **Core Test Access Mode**
  - Core wrapper provides for controlling core inputs and observing core outputs during core test application
  - Test Access Mechanisms (e.g., Test Bus, Test Rail, ...Other) configured during System Chip integration

- **Interconnect & UDL Test Access Mode**
  - Core wrapper provides test observation at core inputs and control at core outputs

- **Test Isolation Mode**
  - Not always required for every core or in every application
  - Can be achieved by constraining core inputs/outputs
  - Protects core and system chip from damage
  - Useful for reducing power consumption, and for Iddq testing
Presentations & Discussions Since ITC98

- Wires Vs Silicon - “Do We Need To TAP our Wrapper?”
- Standard CSP/Wrapper Interface, What Are We Standarizing?
- Living with Shared & Non-Shared P1500 Wrapper Cells
- Benefits and Costs of Shift/Update Flip Flops in a Core Test Wrapper
- Proposed Rules to Resolve Wrapper Cell Dilemma
- Impact of Choosing Wrapper Cell Rules
- Wrapper Cells & Bus Contention
End of Architecture Task Force Status

Feedback and Questions on Status!