Update Presentation of the IEEE P1500 Scaleable Architecture for Testing Embedded Cores

Presented on behalf of the CTAG Team by

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P1500 Architecture Task Force

Active Task Force Members

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Saman Adham - LogicVision
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Mike Collins - Cisco Systems
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Mike Ricchetti - Intellitech
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Paul Soong - Nortel
Jon Udell - Palmchip
Alex Zamfirescu - ASC
Yervant Zorian - LogicVision

★ - Tiger Team Champions
Presentation Outline

- Introduction
- General Update Presentation
- Tiger Team Update Presentations
  - Task Force Mission, Scope and Current Status
  - Overview of Proposed Architecture
  - Core Test Requirements
  - P1500 Architecture Components
  - Agreed To Motions
  - Summary & Future Task Force Activities

**P1500 Architecture Task Force**

*Two Layer Wrapper Development Process*

**Step 1**

Do Wrapper
Serial Interface Layer

**Step 2**

Do Wrapper
TAM Interface Layer
P1500 Architecture Task Force
Serial Interface Layer Tiger Teams

- **Wrapper Instruction Tiger Team**
  - Define and document Wrapper instructions

- **Wrapper Instruction Register Tiger Team**
  - Define and document Wrapper Instruction Register

- **Wrapper Boundary Register Tiger Team**
  - Define and document Wrapper Boundary Register

- **Tiger Teams meet weekly via teleconferencing**
Requirements are the written specification of rules.

Tiger Team

- Identify requirements
- Document requirements
- Modify requirements

CTAG Task Force suggests modifications

Present requirements to CTAG Task Force

CTAG Task Force reviews Tiger Team documents

CTAG accepts requirements

Requirement documents sent to Documentation Group
P1500 Architecture Task Force
General Task Force Status Since ITC99

- Few Discussions on Wrapper Subordination
  - Good idea to support TAMs, e.g. for a BISTed core
  - Need to finalize in WIR Tiger Team

- Memory Discussion
  - General consensus is that memory cores are in P1500 scope & can be easily supported for BIST
  - Will revisit some minor issues after Serial Layer work
  - Would like more input/participation from vendors

- Discussions on “Plug-n-Play”
  - What does it mean to be plug-n-play?
  - Motions on clocking:
    ✓ WIR & Bypass should have dedicated clocks
    ✓ WBR leaning toward allowing system clocks to be used

- Majority of discussion was from Tiger Teams!
P1500 Architecture Task Force

Tiger Team Update Presentations

- Wrapper Instruction Tiger Team Update
  - Teresa McLaurin

- Wrapper Instruction Register Tiger Team Update
  - Mike Ricchetti

- Wrapper Boundary Register Tiger Team Update
  - Jason Doege